A Project Report

on

Process-in-Loop Analysis of Universal Control Technique for a Hexagonal-Shaped Reduced Device Multilevel Inverter

in partial fulfillment for the award of the degree

of

BACHELOR OF TECHNOLOGY (B. TECH)

IN

ELECTRICAL ENGINEERING

Submitted by:

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(A Govt. Aided UGC Autonomous & NAAC Accredited Institute, Affiliated to RGPV Bhopal)

MAY 2023

CANDIDATE'S DECLARATION

I hereby declare that the project titled **"Process-in-Loop Analysis of Universal Control Technique for a Hexagonal-Shaped Reduced Device Multilevel Inverter"** submitted for the award of **Bachelor of Technology** degree in **Electrical Engineering** is my original work and the project has not been submitted elsewhere for the award of any other degree, diploma, fellowship, or any other similar titles.

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Place: Gwalior

Date: 20 May 2023

This is to certify that the above statement made by the candidate is correct to my knowledge and belief.

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ABSTRACT

Abstract— An electrical device used for converting DC voltage into AC voltage with multiple voltage levels is termed as multilevel inverter. Unlike conventional inverters that generate square-wave or pulse-width modulated waveforms, multilevel inverters produce a stepped waveform with several voltage levels. The main advantage of multilevel inverters is their ability to lower the output waveform's harmonic content, resulting in reduced stress on the load and improved efficiency. They are also useful in applications where high voltage or high power output is required. Their main drawback is complexity, as they need a lot of batteries and switches. This article introduces a novel fifteen-level inverter with an asymmetric hexagonal design and uses MATLAB simulation to study the analysis of THD and harmonics The universal control scheme is tested experimentally using STM32F4 discovery board and proposed MLI configuration has been tested using various PWM techniques. It first aims to reduce the number of components. Additionally, it uses a small number of switching devices to produce each level of output voltage and has a low total device rating (TDR) and total blocking voltage (TBV). In comparison to traditional multilevel inverter topologies, the proposed topology uses only eight switching devices to give fifteen levels at the output.

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LIST OF ABBREVEATIONS

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1. MLI – Multilevel inverter
2. PWM- Pulse Width Modulation
3. THD – Total Harmonics Distortion
4. MI- Modulation Index
5. TDR- Total device rating
6. TBV- Total Blocking Voltage

CHAPTER I: INTRODUCTION

The first multilevel inverter (MLI) was introduced in 1975, since its invention, demand for DC/AC power conversion and related applications has been rapidly increasing [1]. Three level is the basic building block of a multilevel inverter; it like a square waveform [2]. Multilevel level inverter is widely used for medium and high power systems, because it provides high quality output waveform with low harmonic distortion.

MLIs are often divided into three categories: Flying capacitor (FC), Neutral point clamped (NPC), and cascaded H-bridge (CHB). Most published material over the last few decade's studies CHB, FC, and NPC topologies in terms of their individual benefits and drawbacks [3]. NPC (Neutral Point Clamped Inverter) topology, also referred to as diode-clamped topology, first gained attention when Nabae et al. demonstrated the use of an NPC inverter during experimentation utilising a pulse-width modulation technique in the 1980s. The clamping diode is used for the Diode-Clamped Multilevel Inverter to transmit a minimal quantity of voltage. N^2 is the total number of components needed for N level voltage generation, which includes (N-1)*(N-2) clamping diode, 2 (N-1) switching devices linked in series, (N-1) dc link capacitor to split the dc link into various voltage levels, and one dc source. Diode clamped Multilevel inverters have a significant disadvantage in that only half of the input dc voltage is produced by them at their peak voltage, but they also have high efficiency due to the fundamental frequency that is used in all switching devices. Flying Capacitor Multilevel inverter's configuration structure is similar to that of the preceding one, with the exception that here, capacitors are employed to limit voltage rather than diodes. In order to limit voltage, n level flying capacitor inverters combine (n-1) *(n-2)/2 flying capacitors with (2n-2) switching components.

The cascaded H-bridged multi-level inverter (CHBMLI), one of the common types used in high power moderate voltage circuits, is one such device. There are several cascaded H-bridge multi-level inverters topologies depending on the input DC voltage source. The first type of CHBMLI has equal DC voltage supplies; this form of inverter generates high ac voltages by combining several equal units of the power supply [10]. And the term "classical topologies" is now frequently used to describe these topologies. The conventional topologies don't likely to have much that is advantageous as application and component count, complexity, and cost considerations have

a significant impact on multilevel solutions. Because of its modularity and simplicity among the traditional MLI, CHB has drawn a lot of attention; yet, the topology limitation is a requirement of an isolated source. [4]. As a result, many topologies and control schemes have been presented in recent years with a lower device count that combine unidirectional and bidirectional switches of various ratings [5-6]. There have been several reduced switch MLI topologies introduced, and they largely are divided into two categories: MLI topologies that are symmetric and asymmetric [7]. Anoop suggested a topology for a fifteen-level inverter, using three capacitors, sixteen diodes, and sixteen semiconductor components to generate the fifteen levels of output voltage. Due to the existence of capacitor devices and the high component count in this design, ripple voltage issues exist [8]. Anand also proposed a fifteen-level asymmetric inverter [9]. While using a comparatively smaller number of switching devices than [10], still uses a huge amount of components. To address the current problems, the smallest number of components possible asymmetric multilevel inverter topology had been introduced. In order to address these issues, a novel fifteen-level inverter with a hexagonal design is presented in this paper.

The advantage of the suggested topology is that fewer components are needed: For generating fifteen output levels, it consists of a diode, three voltage sources, and eight switching devices. The proposed modulating signal reduces the no of active switches as well as total number of components required for generation per level output voltage. And this topology is extendable up to n level

1.1 Objective

In order to overcome the problem of distortion in the output voltage waveform caused due to the presence of harmonics, this project proposes Universal Control Scheme on a Fifteen Level Inverter topology using MATLAB/SIMULNIK 2016a. The objectives of the work are:

1. To study and simulate a Single-Phase fifteen level voltage source inverter (VSI).
2. Comparison of proposed topology with the original existing topologies.
3. Comparison of THD (Total Harmonic Distortion) in different control techniques.
4. To understand and implement Pulses Width Modulation to reduce the need for filtering

1.2 Problem Formulation

1. In high-power and high-voltage applicants low-level (for eg. Three , five, seven) inverter have some limitations in operating at high frequency.
2. Total harmonic distortion (THD) is a significant component of low-level inverters.
3. Low-level inverter doesn't provide good quality of output waveforms.
4. No of switching component are large in other conventional topologies

1.3 Solution Methodologies

Implementation of a 15-level inverter to mitigate the drawbacks of low-level inverter use:

1. Increasing the level of inverter will make the resultant waveform move toward the sinusoidal waveform. Increasing the waveform quality.
2. The proposed topology employs less number of DC voltage source to produce high level voltages and less number of switching devices which also reduces the switching losses.
3. With minimal overall harmonic distortion and no need for a transformer, the proposed Topology of the multilevel inverter enables high voltage levels.

1.1 Inverter

Most of the household appliances along with other electrical equipment and fixtures purely depend on AC electricity. Energy demand is increasing day by day globally due to economic growth and cooling and heating demand. The major concern across the world is fossil fuel expenditure and its availability. Humankind is facing two major problem currently: the environment climate crisis and energy crises. Due to these reason we are moving towards Renewable energy sources. Many countries are working on green energy sources. Most of the renewable sources produces DC power. In grid connected system it is necessity to convert it in AC. Inverter is a device that convert DC into AC.

1.2 Multilevel Inverter Types

There are three main types of multilevel inverters:

1.2.1 Diode Clamped MLI

Diode-clamped topology, also referred to as NPC (Neutral Point Clamped Inverter) topology, first drew attention when Nabae et al. demonstrated the use of an NPC inverter alongside experimentation utilizing a pulse-width modulation technique in the 1980s.

The clamping diode is used for the Diode-Clamped Multilevel Inverter to transmit a minimal quantity of voltage. n^2 is the total number of components needed for n-level voltage production, which includes 2*(n-1) IGBT devices linked in series, (n-1)*(n-2) clamping diodes, (n-1) dc link capacitors to split the dc link into various voltage levels, and one dc voltage source . Diode clamped multilevel inverters have a significant disadvantage in that their maximum output voltage is only half of the input dc voltage, but they also have high efficiency due to the fundamental frequency that is used in all switching devices.

1.2.2 Flying Capacitor MLI

This inverter's configuration structure is similar to that of the preceding one, with the exception that here, capacitors are employed to limit voltage rather than diodes. In order to limit voltage, n level flying capacitor inverters combine (n-1) *(n-2)/2 clamping capacitors and (n-1) DC link capacitors with (2n-2) switching components.

1.2.3 Cascaded H-bridge Inverters

The cascaded H-bridged multi-level inverter (CHBMLI) is one of the popular forms of multi-level inverters utilized in high power moderate-voltage circuits. There are several topologies for cascaded H-bridge multi-level inverters with regard to the input DC voltage source. The first kind of CHBMLI has equal DC voltage supplies; this form of inverter generates high ac voltages by combining several equal units of the power supply.

1.3 Advantages of MLI

- Total harmonic distortion (THD) reduces

- High Voltage level obtained
- Staircase waveform quality
- Operates at both fundamental and high switching frequency PWM
- Low switching losses
- High power quality
- Electromagnetic interference reduces.
- They generate less CM, or common-mode voltage. Furthermore, CM voltages can be eliminated using complex modulation techniques.

1.4 Applications

- High-voltage and Medium-voltage motor drives.
- High voltage dc transmission.
- Flexible AC transmission system (FACTS).
- Traction
- Active filtering
- Utility interface for renewable energy systems.

CHAPTER II: PROPOSED HEXAGONAL SHAPED MULTILEVEL INVERTER

In this study, a special multilevel inverter structure with a hexagonal shape has been proposed. In this configuration, there are three dc-link voltages, one diode, and eight switching devices to provide an output voltage with fifteen levels (Fig. 1). The computation of blocking voltage has been briefly discussed below.

2.1 OPERATING PRINCIPLE

The proposed topology's basic idea is demonstrated in this subsection. Seven positive modes, seven negative modes and a single zero mode make up the proposed topology's fifteen modes. The suggested structure requires just eight switching devices and three voltage sources to provide these fifteen modes. The voltage sources' values are selected in such a way that V2 and V3 must be two and four times the supply voltage respectively. To avoid a short circuit of dc sources, the switches (S3, S6) and (S1, S2) are all turned on simultaneously. Table1 provides an illustration of how this suggested topology functions. Fig.2 presents some voltage generation techniques.

Table 1. Switching states of the proposed topology

Voltage level	Active switch	Current path
V1+V2+V3	T2,T8,T4,T6	V3-T2-V1-T8-V2-T4-LOAD-T6-V3
V2+V3	T2,T4,T6,T7	V3-T2-T7-V2-T4-LOAD-T6-V3
V1+V3	T2,T4,T6	V3-T2-V1-D1-T4-LOAD-T6-V3
V3	T2,T1,T6	V3-T2-T1-LOAD-T6-V3
V1+V2	T8,T4,T3,T2	V1-T8-V2-T4-LOAD-T3-T2-V1
V2	T4,T3,T2,T7	V2-T4-LOAD-T3-T2-T7-V2
V1	T4,T3,T2	V1-D1-T4-LOAD-T3-T2-V1
0	T4,T5,T6	T4-LOAD-T6-T5-T4
-V1	T5,T6,T1	V1-D1-T5-T6-LOAD-T1-V1
-V2	T7,T5,T6,T1	V2-T5-T6-LOAD-T1-T7-V2
-(V1+V2)	T5,T6,T1,T8	V1-T8-V2-T5-T6-LOAD-T1-V1
-V3	T3,T4,T5	V3-T3-LOAD-T4-T5-V3
-(V1+V3)	T5,T3,T1	V1-D1-T5-V3-T3-LOAD-T1-V1
-(V2+V3)	T5,T3,T1,T7	V2-T5-V3-T3-LOAD-T1-T7-V2

-(V1+V2+V3)	T5,T3,T1,T8	V1-T8-V2-T5-V3-T3-LOAD-T1-V1

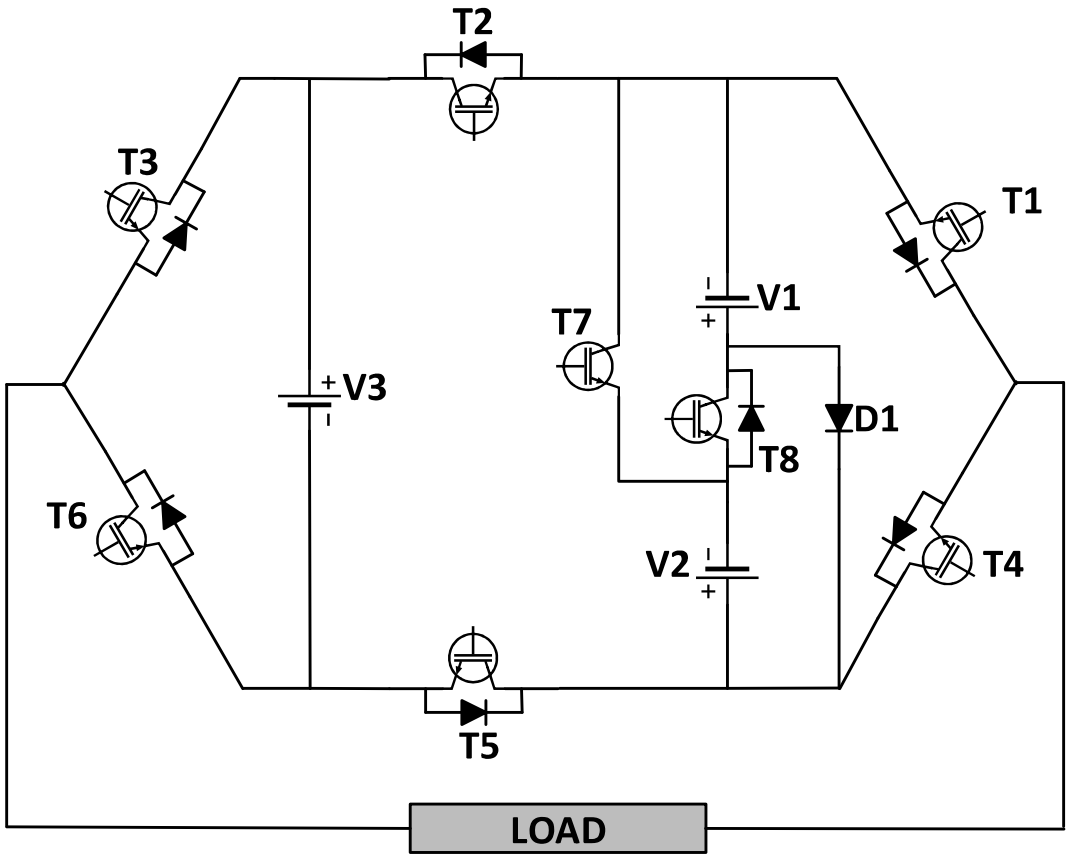
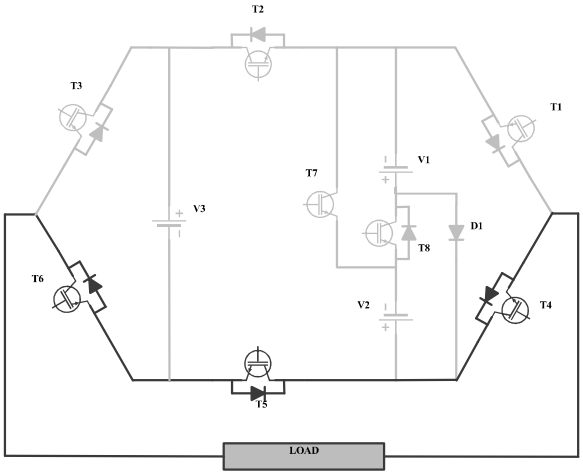


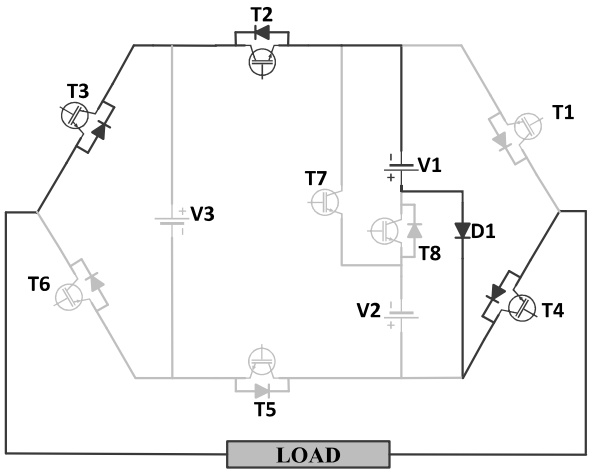
Fig. 1. Proposed hexagonal-shaped multilevel inverter**.**

2.2 OPERATING STAGES

The following figures illustrate different operating modes used to achieve various voltage levels.



(i)



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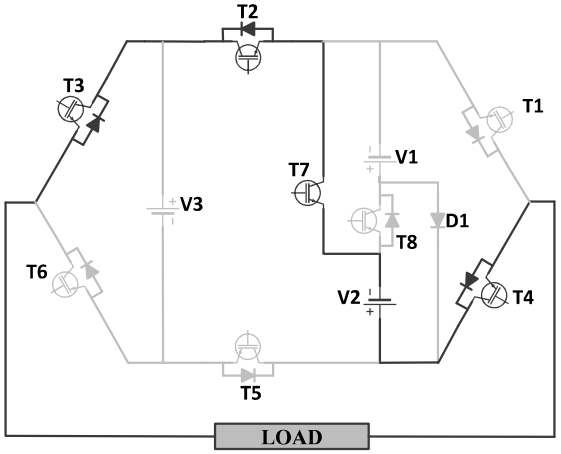

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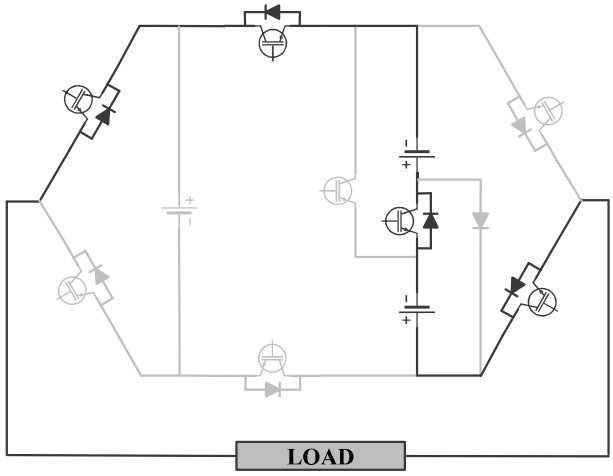

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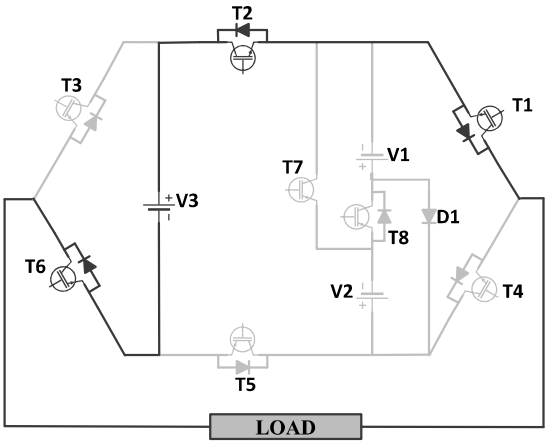
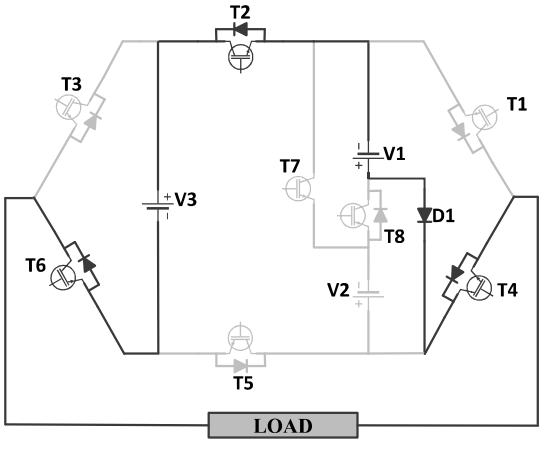


(v)



(vi)

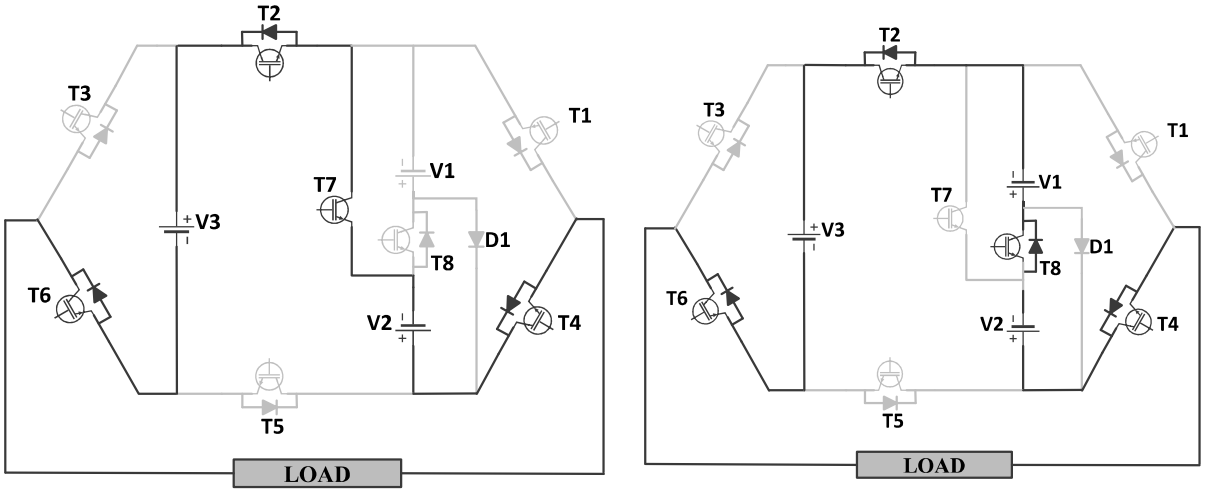


Fig. 2. Procedures for generating output voltage levels: (i) 0; (ii)V1; (iii)V2; (iv)V1+V2 ; (v)V3; (vi)V1+V3; (vii)V2+V3; (viii)V1+V2+V3

2.3 Universal Control Technique

In this section, the suggested universal control technique is explained. It can be used with any multilevel inverter topology because of the way it is designed. Let the total number of level in the phase voltage for the supplied inverter will be N level .If N level is greater than 3, a voltage source inverter can function at various waveform's number of positive levels will also be:

$$N= (N_{level} -1)/2$$

A sinusoidal waveform of amplitude A_{ref} and frequency f_{ref} constitutes the modulating signal $s_{ref}(t)$ [11]. For sine PWM and low-frequency schemes, there needs to be triangular, constant, 2N carrier signals. The frequency of these carriers is f_{ref} and A_{car} is their peak-to-peak amplitude. Carrier signals that are higher than the zero level are known as $s^{+}_{car,j}(t)$ and those that fall below the zero level are known as $s^{-}_{car,j}(t)$, (j = 1 to N). The zero reference is positioned in the middle of the continuous bands that the carrier signals occupy.

Accordingly, the following quantities can be defined:

Index of frequency modulation , P= w_{car}/w_{ref}

"P" determines the output waveform's harmonic profile as well as the power switches' switching frequency.

Index of amplitude modulation, M=$A_{ref}/(N\ A_{car})$

The output waveform's peak value and number of levels are determined by the value of "M".

Every time, the modulating signal is compared to each carrier [14]. For each comparison, the outcome is either "1" if the modulated signal exceeds the carrier, or "0" otherwise. All carrier signals above the zero reference are affected by this. For each comparison, the outcome is either "0" if the modulating signal exceeds the carrier or "-1" if the carrier signal falls short of the zero reference.That is.

$s^{+}_{out,j}(t) = 1,\ for\ s_{ref} \geq s^{+}_{car,j}(t)$ = 0, otherwise

$s^{-}_{out,j}(t) = 0,\ for\ s_{ref} \geq s^{-}_{car,j}(t)$

= -1, otherwise

The results so obtained are combined to create an "Aggregated signal" that is designated as $\boldsymbol{s_{agg}(t)}$.That is,

$$s_{agg}(t) = \sum_{j=1}^{N} (s^{+}_{out,j}(t) + s^{-}_{out,j}(t))$$

It should be observed that the waveshape of $c_{agg}(t)$ gains the same property as the expected output voltage. With a certain topology, power electronic switches require real-world driving signals, which requires the use of logical components and a look-up table to be generated from $s_{agg}(t)$. Using Boolean operations,

$$s_{d,t}(t)\ are\ derived\ from\ s_{agg}(t)\ using\ following\ criteria:$$

$s_{d,t}(t) = 1, if\ s_{agg}(t) = j$

$= 0, otherwise;\ where, j = -N\ to\ +N$

As a result, there will be a total of N level derived signals, each of which will be used to operate the switches that must remain ON at the voltage level indicated by the output waveform. In order

to acquire the switching function $s_{switching}(t)$ for a certain switch, the necessary derived signals would be sent into an OR gate. The mathematical formulation of the switching function is

$$s_{switching}(t) = \overline{\prod \overline{s_d(t)}}$$

Where,

$$\overline{s_d(t)} = 1 - s_d(t)$$

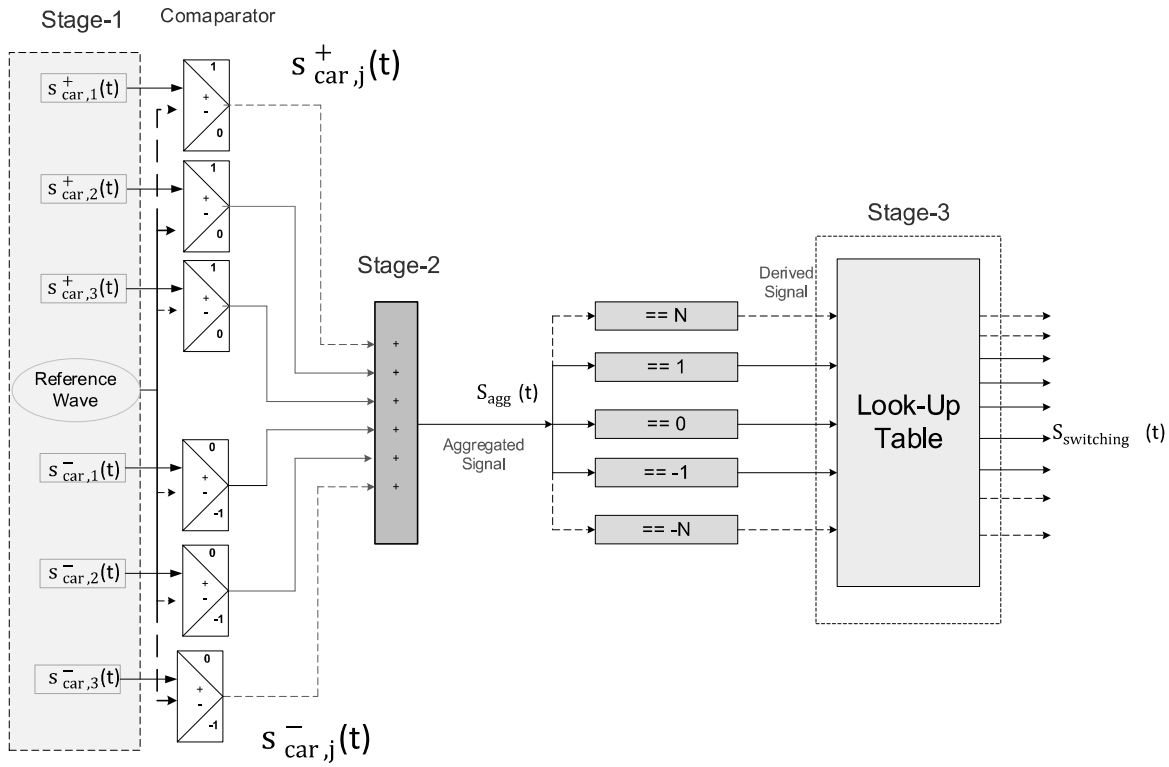


Fig.3 Block Diagram of Universal Control Scheme

2.4 Calculation of Blocking Voltage

Designing multilayer inverters requires careful consideration of the blocking voltages on the switching devices. Therefore, the problems with blocking voltage have a significant impact on the price and size of multilevel inverters. When a switch is reverse biased, blocking voltage

appears across it. The total blocking voltage in a topology is the sum of the individual blocking voltages needed for each switch. For the suggested topology, we may obtain the following equation for total blocking voltage:

$$V_{blocking} = VS1 + VS2 + VS3 + VS4 + VS5 + VS6 + VS7 + VS8 \quad (1)$$

Equation (1) results in a total blocking voltage of 28 V, where V is the minimum dc-link voltage.

CHAPTER III: CONTROL AND MODULATION TECHNIQUES IN PROPOSED TOPOLOGY

For MLIs, various types of modulation techniques have been proposed in the literature. Multiple carriers, which can be saw-tooth or triangular signals, are used in multilevel carrier-based PWM techniques. The following properties of carrier signals are open to change: frequency, amplitude, phase of each carrier, and offset between the carriers. Additionally, the reference wave (modulating signal) allows for injection of zero sequence signals as well as freedom in frequency, amplitude, and phase angle. So many multilevel carriers-based PWM techniques can be obtained by applying these combinations. In general, it would be necessary to have a set of n-1 carrier signals for an inverter with n-levels in the phase voltage [15].
The multicarrier pulse width modulation techniques are as follows

A. Phase Disposition (PDPWM) PWM

All carriers' signals in this technique are level shifted and phase shifted. The carrier set's zero reference is positioned in the Centre. A set of phase-disposed carrier waveforms for a 15-level inverter used to generate pulses can be seen in Fig.4.

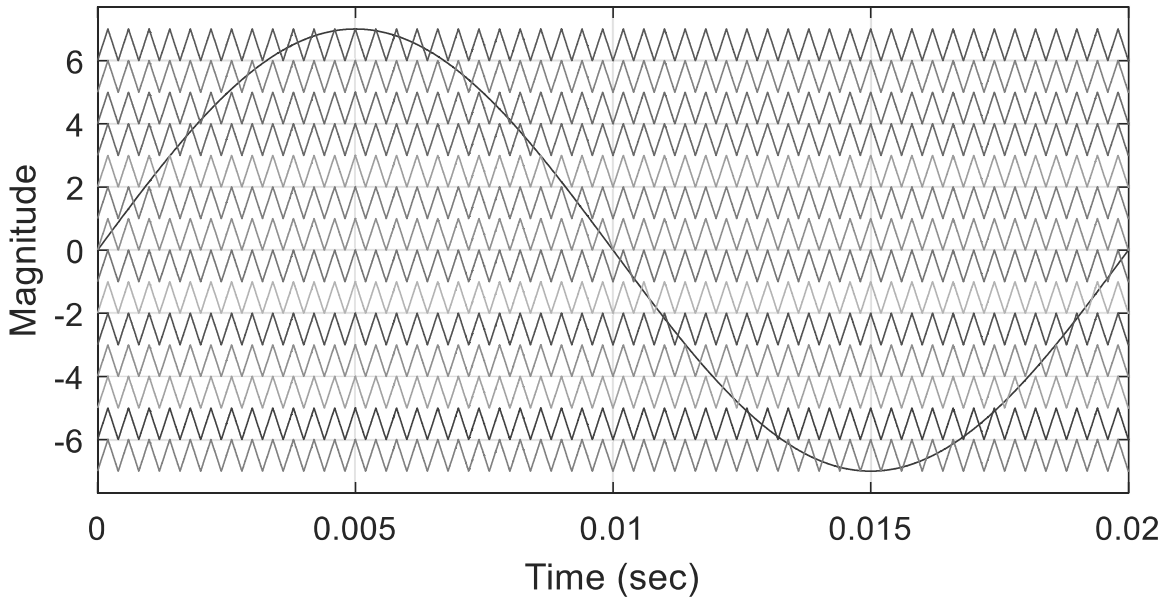


Fig.4 PD technique

B. Phase Opposition Disposition (PODPWM) PWM

In this method, the carrier signals above and below the zero reference are in phase with one another, but they are 180 degrees out of phase, respectively.as shown in Fig. 5.

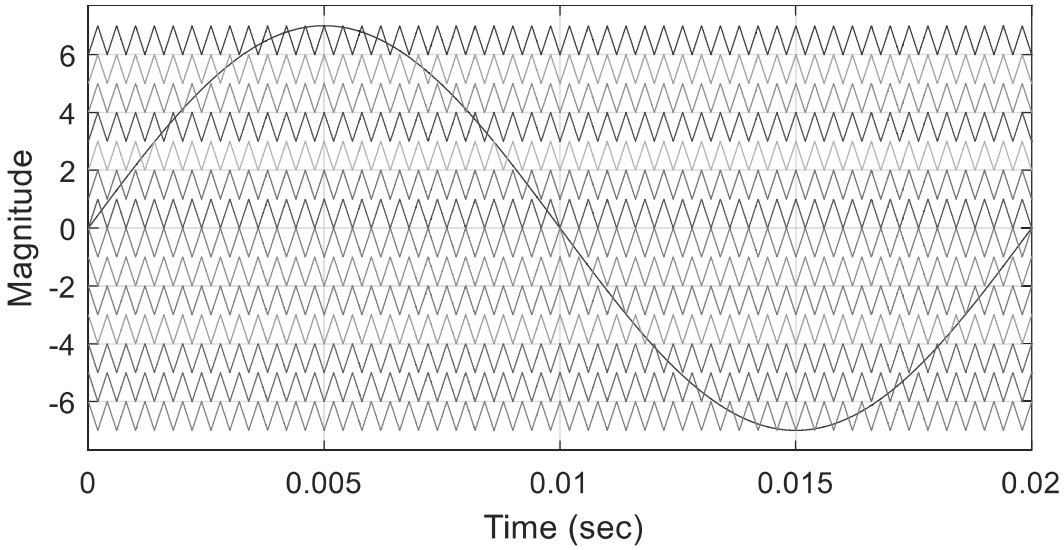


Fig. 5 POD technique

C. Alternate Phase Opposition Disposition PWM (APODPWM) Technique.

The carrier signals in this technique alternately phase-displace by 180 degrees from one another, as shown in Fig.6.

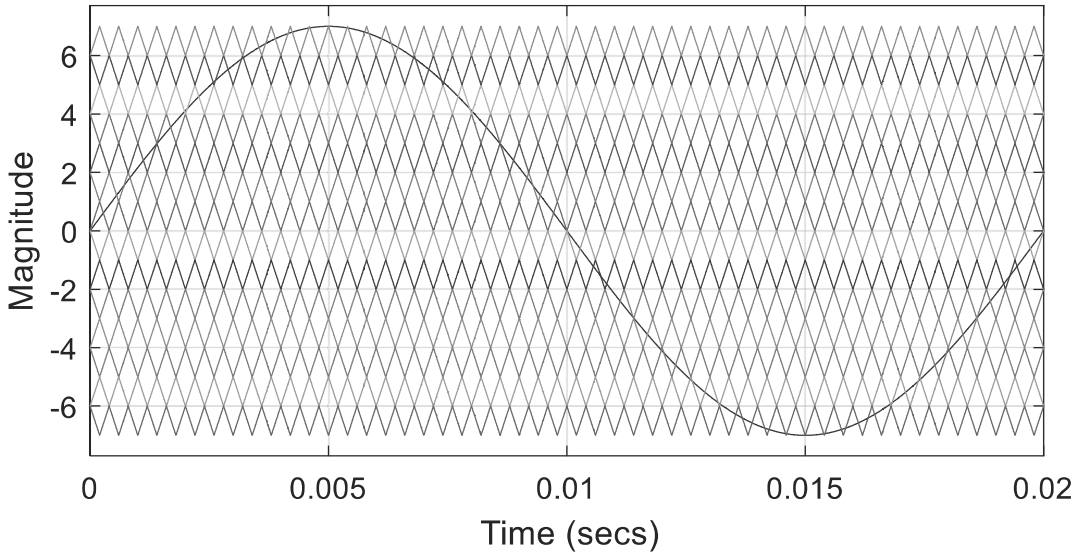


Fig. 6 APOD Technique

D. Variable Frequency Inverted sine carrier PWM (VFISCPWM) Technique

In this technique, the reference wave is an inverted sine wave with variable frequency, and the sine wave is used as the carrier wave, with the carrier signals having different frequencies from each other. Whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave, pulses will be generated using the control technique as shown in the Fig.7.

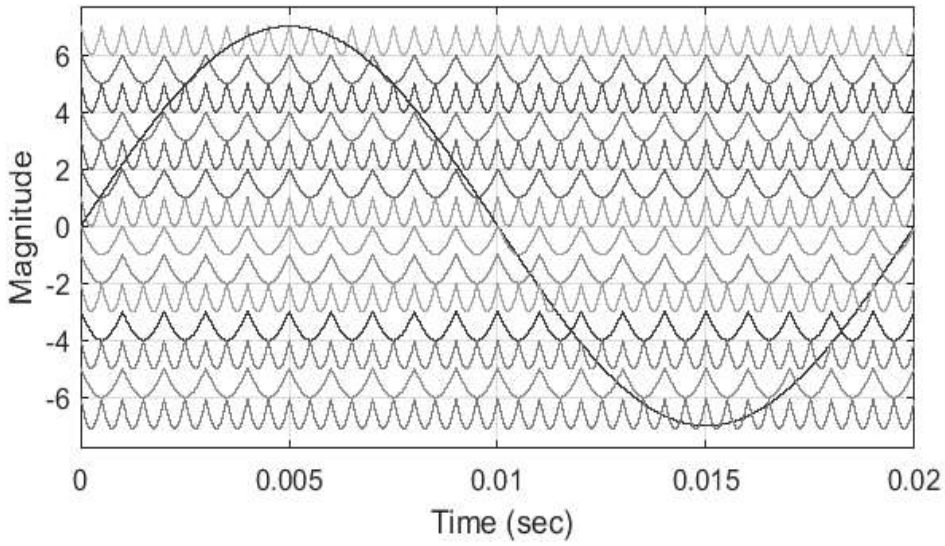


Fig.7 VFISC Technique

E. Inverted Sinusoidal Carrier (ISCPWM) PWM

The carrier wave in this technique is a sine wave. In the inverted sine carrier PWM (ISCPWM) technique reference signal is a sine wave and an inverted sine carrier with a high frequency as the carrier signal. Combining reference and carrier signals with various modulation indexes results in low harmonic distortion.

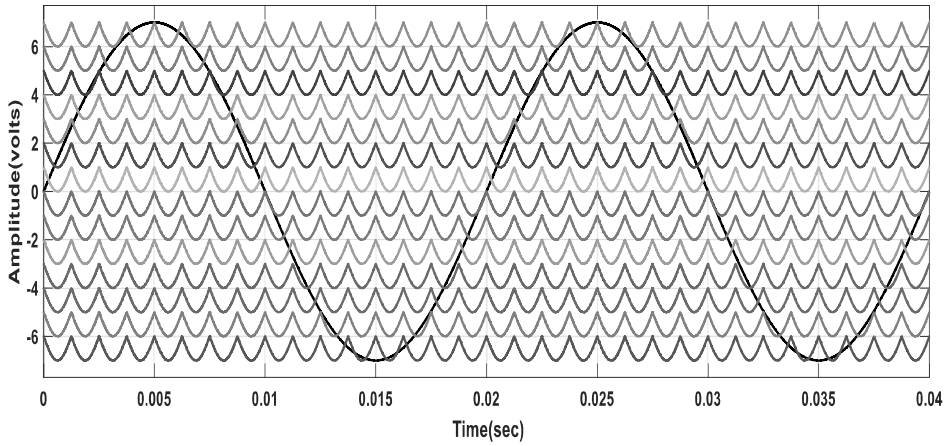


Fig. 8 ISC Technique

CHAPTER IV: SIMULATION AND EXPERIMENTIAL RESULT

4.1 SIMULATION RESULT

MATLAB/SIMULINK R2016a is used to simulate this proposed multilevel inverter topology. The following are the simulation's parameters: R=10 with dc voltage V1 = 100V, V2=200V and V3=400V .The switches has been assumed ideal and carrier signal frequency is 10kHz and this paper has five PWM techniques are used PD,POD,APOD ,ISC and VFISC with different Modulation Index (MI)[13] .THD of five PWM technique are shown in table 2. In MATLAB/Simulink, the harmonic spectrum is determined via FFT analysis.

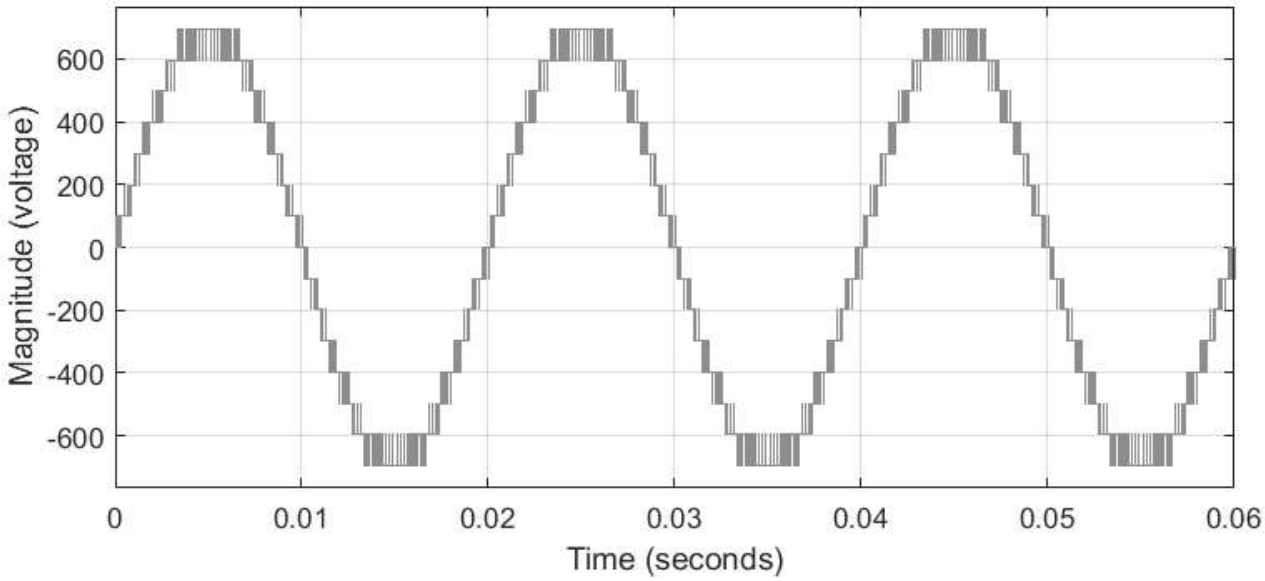


Fig. 9 Output voltage waveform of 15-level MLI

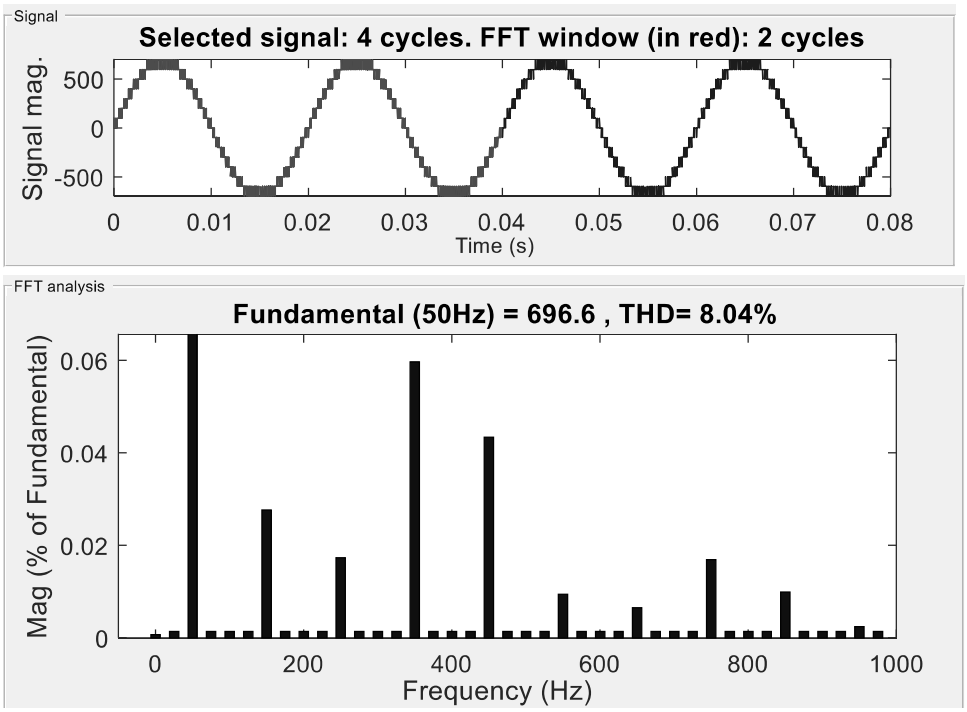


Fig.10 THD of 15-level MLI with APOD technique and MI 1.

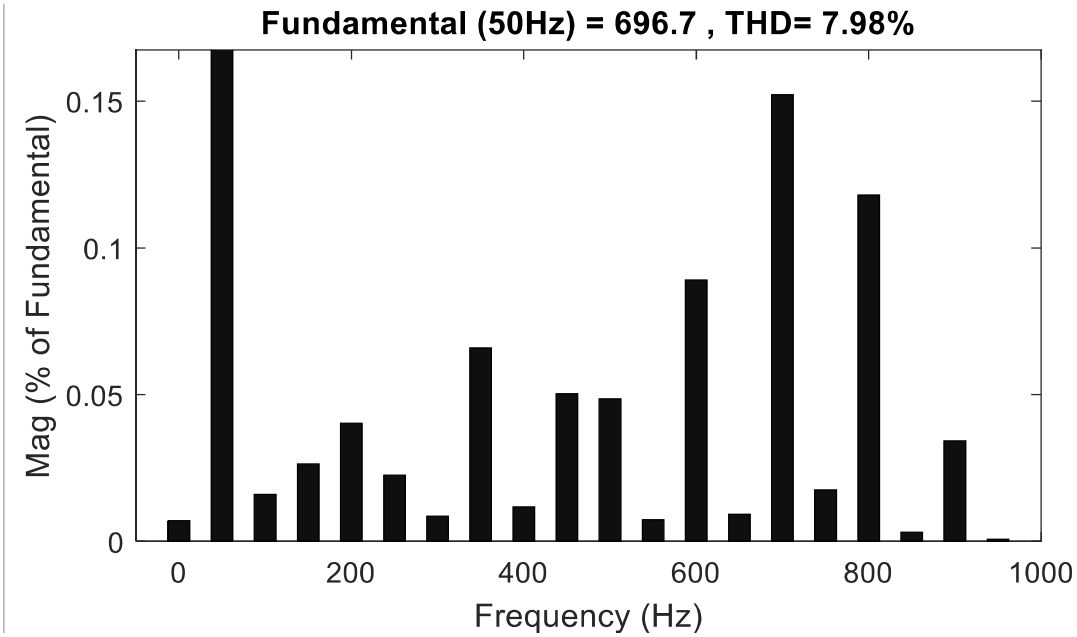


Fig.11 THD analysis with PD technique and MI 1.

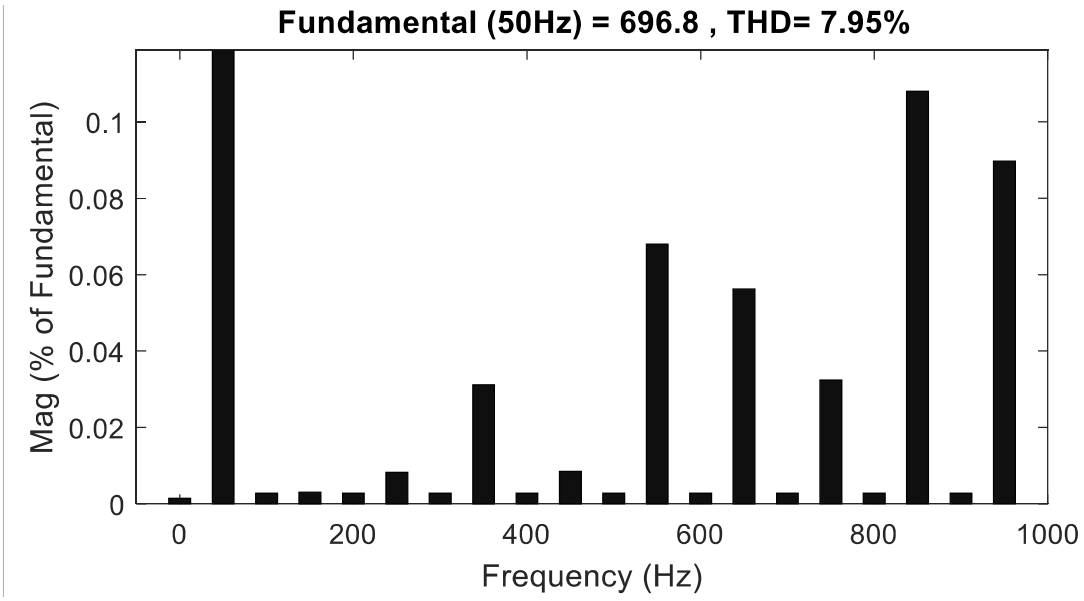


Fig.12 THD analysis with POD technique and MI 1.

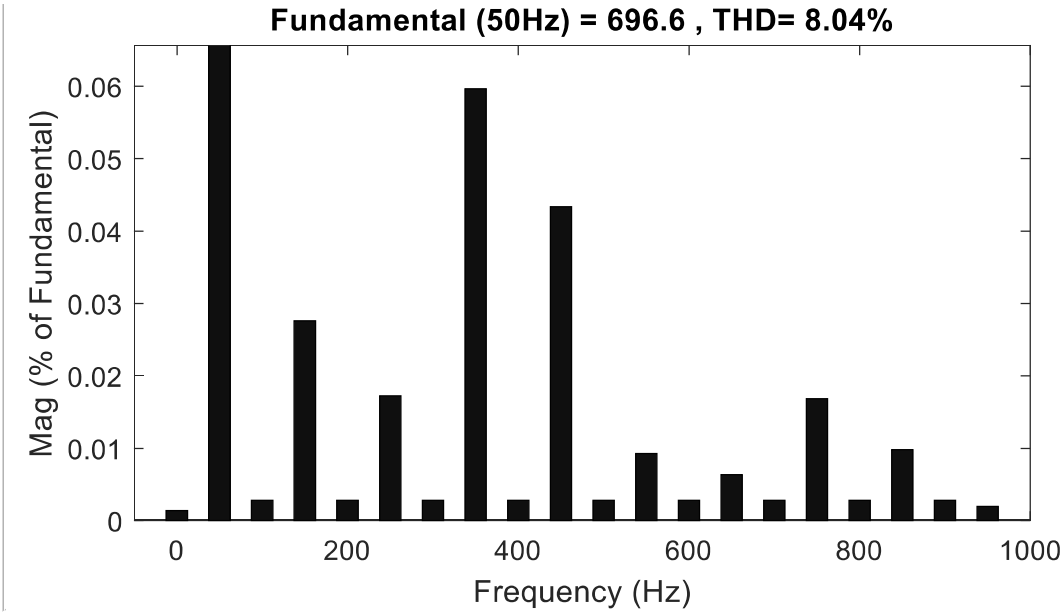


Fig.13 THD analysis with APOD technique and MI 1

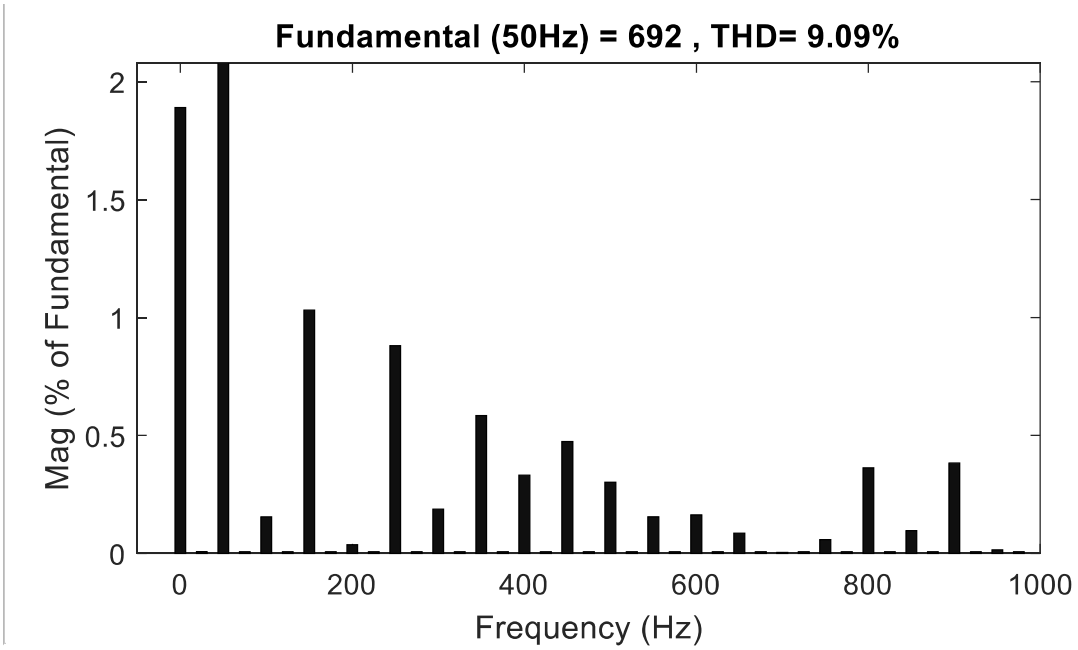


Fig.14 THD analysis with VFISC technique and MI 1.

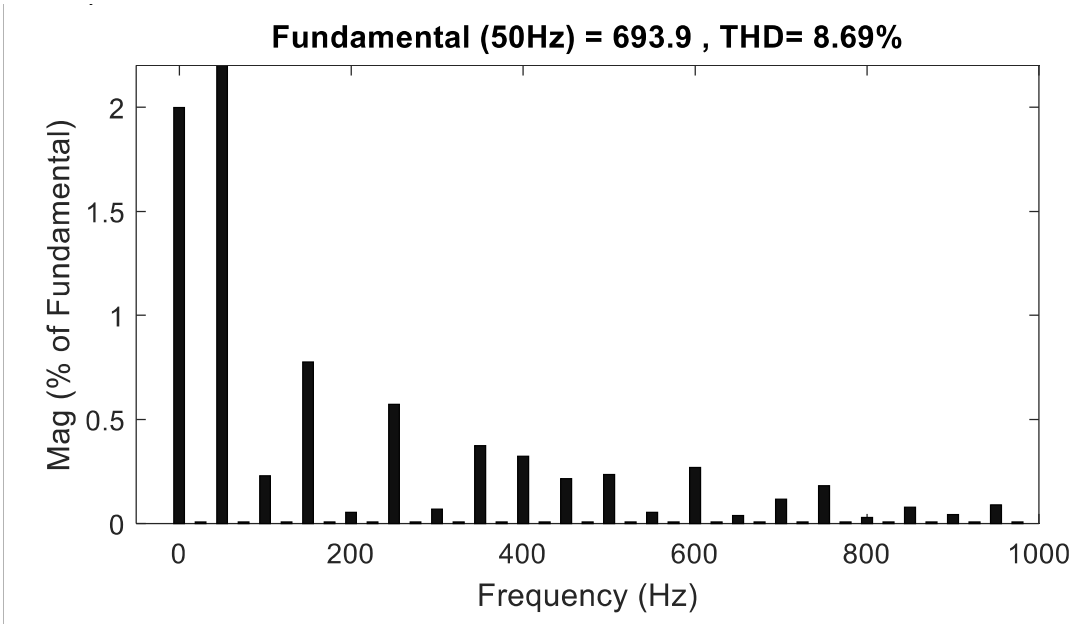


Fig. 15 THD analysis with ISC technique and MI 1.

Table.2: Comparison of different modulation technique results

Level	Modulation Index	Modulation Technique				
		PD	POD	APOD	VFISC	ISC
15 level	1.1	7.61	7.55	7.59	8.07	7.85
	1	7.98	7.95	8.04	9.09	8.69
	.9	9.03	9.01	8.89	9.77	9.50
	.8	10.65	10.65	10.67	11.21	11.01

Table.3: Comparison of multiple MLI topology

Inverter Topologies	CHB	NPC	Flying-Capacitor	Proposed Topology
IGBTs/Switching Devices	28	28	28	8
Diodes	0	0	0	0
Clamping diode	0	182	0	0
DC bus capacitor	0	14	14	0
Flying capacitor	0	0	91	0
Dc source	7	1	1	3

4.2 EXPERIMENTAL RESULT

In the paper, the universal control techniques have been implemented to control the MLI. Five different PWM modulations techniques have been presented on varying modulation index. In experimentation, a low cost STM32F4 discovery board haven been used to verify universal technique experimentally. The experimental photograph is shown in figure 16. The discovery board is fitted with ARM Cortex –M4 32 bit microcontrollers and have fifteen analog to digital pin (PA0-PA7,PB0-PB1 and PC0 to PC5) , two digital to analog pins (PD0-PD1),. In this paper DAC pins are used to extract the outputs of multilevel inverter. Real-time implementation of created Simulink models can be readily created and loaded into the board memory by using Keil, embedded coder target for STM32F4, and other working tools.

Create a model using Simulink that includes embedded target blocks in accordance with the applications and accessibility requirements. Before creating any files for Simulink models, ensure that the primary directory path is correctly located in MATLAB's command window. Simulink models can be created and executed on a discovery kit by using the Support packages for STMicroelectronics' STM32F4 exploration board. Simulink blocks for configuring and gaining access to board peripherals are included in the support package. The STM32F4 blocks' third-party interface, in addition to MATLAB, is Waijung software. To complete the Waijung block installation, the user needs install the STM link utility driver. Choose the parameter parameters for the target arrangement based on your requirements. FIG. 17-19 displays the experimental findings at various modulation indices.

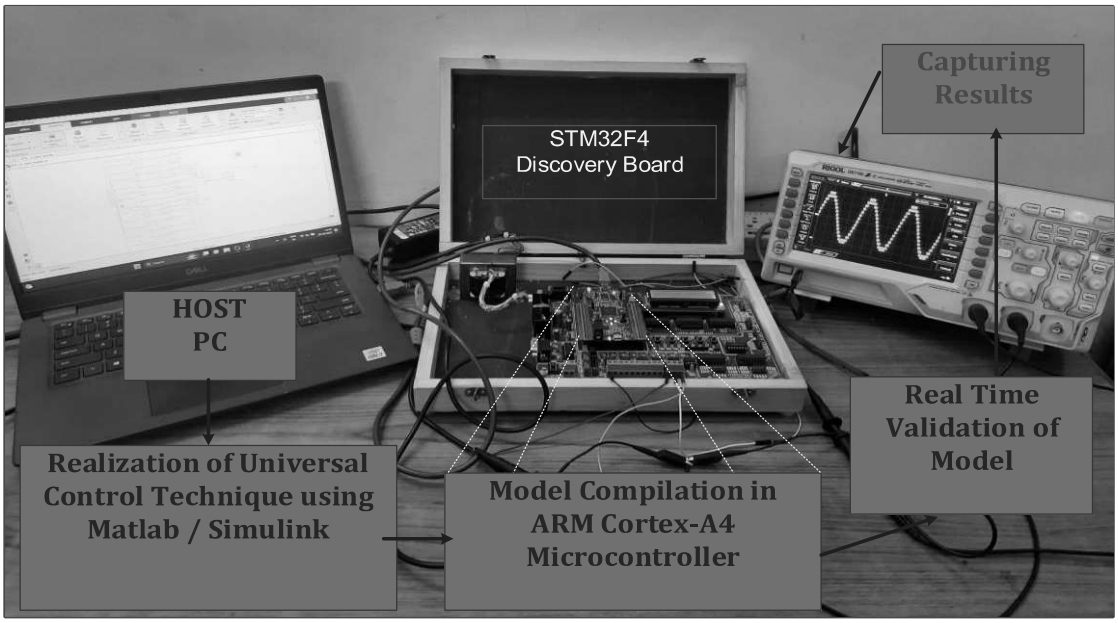


Fig.16 Experimental Realization of Universal Control Technique

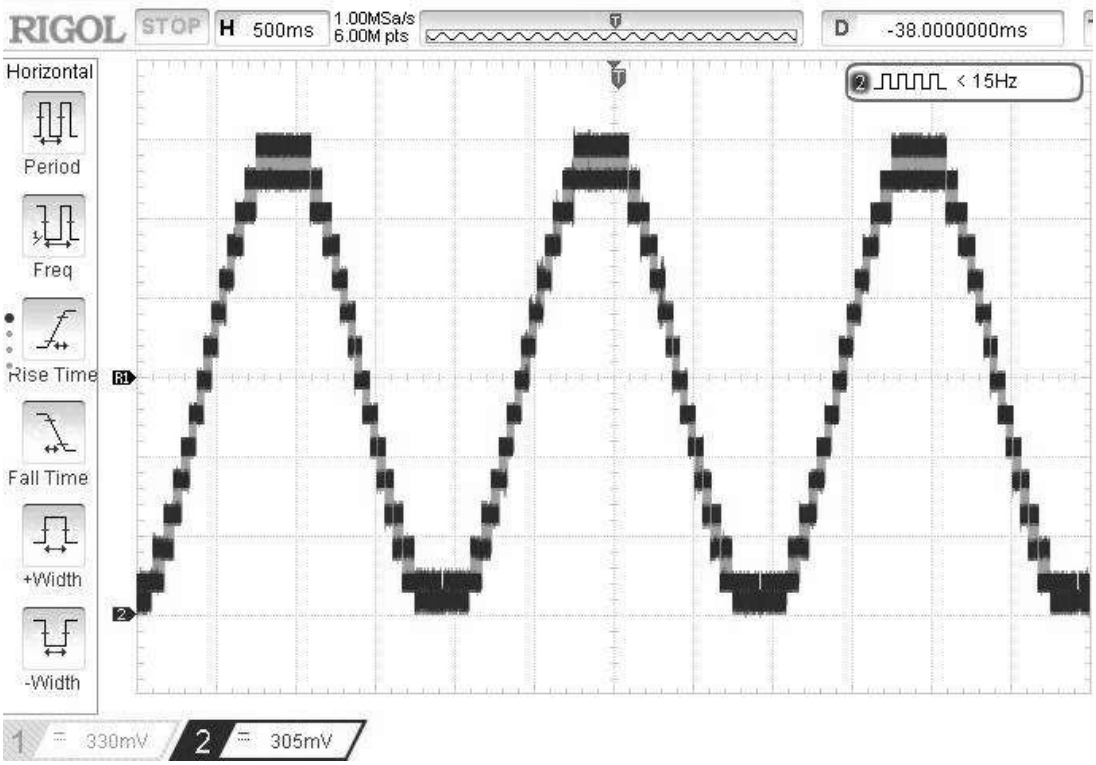


Fig.17 Modulation index (MI) 1.

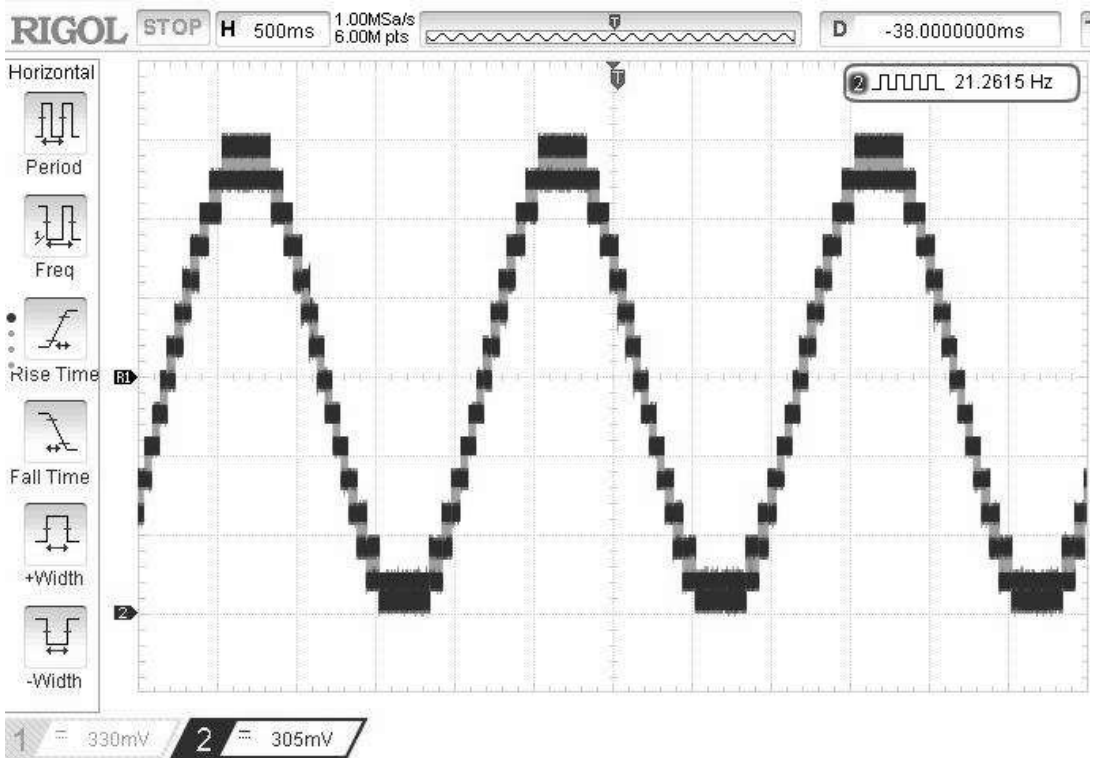


Fig.18 Modulation Index (MI) 0.8

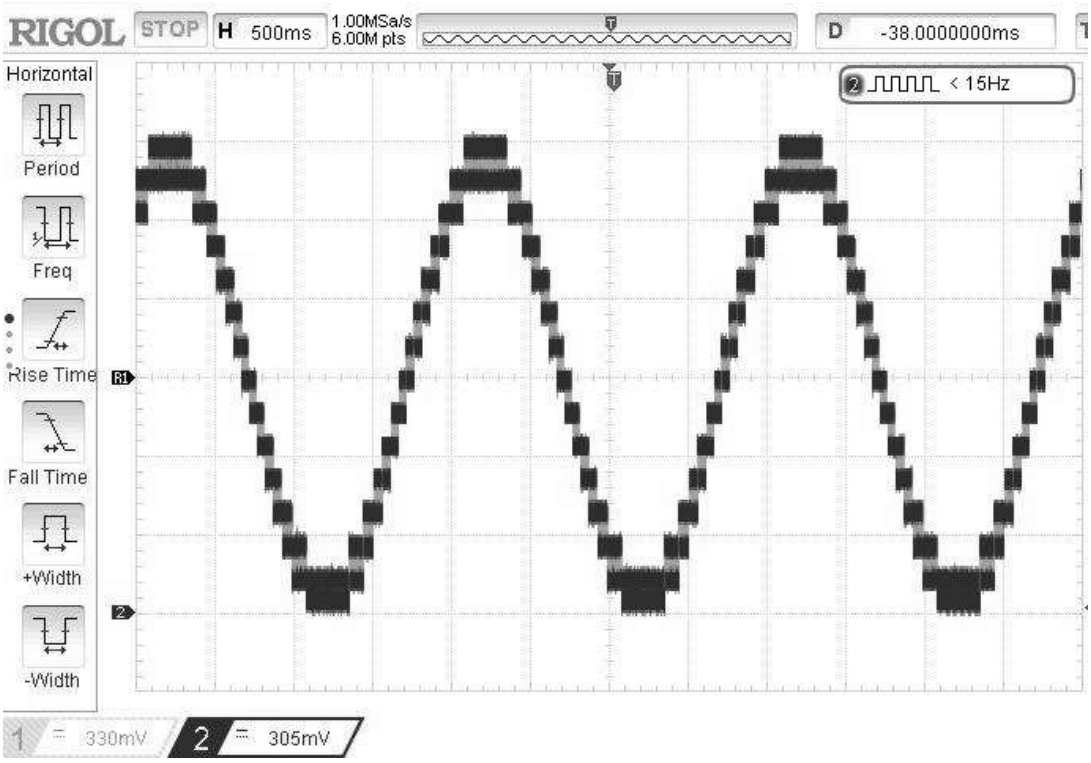


Fig.19 Modulation Index (MI) 0.6

CHAPTER V: CONCLUSION

In place of the traditional multilevel inverters, a new fifteen-level inverter with a hexagonal design was introduced in this study for the grid-integrated system. The number of components was decreased by the suggested topology. Moreover, it ensures the lowest hardware implementation cost. The suggested inverter topology is controlled by switching pulses produced by the low-frequency modulation approach, which also offers the lowest total harmonic distortion. There is no need for a filter with the suggested inverter. Consequently, in the future power system, the grid-connected systems are made more reliable, efficient, and compact due to the proposed inverter topology. The simulation outcomes for an inverter with a 15-level hexagonal design have been given. It was shown that the inverter's THD varies when different PWM techniques are applied, and the Phase Opposition Disposition (POD) Method achieves the lowest THD. Reduced device multilevel inverters have the potential to revolutionize various sectors, including renewable energy, transportation, industry, and power quality. Continued research and development efforts in this field are likely to lead to further advancements, improved performance, and increased adoption of these inverters in future energy systems.

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Appendix

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1 message

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Reply to: Saurabh Kumar Rajput <saurabh9march@gmail.com>
To: Akash Kushwah <akashkushwah47ak47@gmail.com>
Cc: saurabh9march@mitsgwalior.in

Dear Authors
Thanks for submitting your research paper to International Student Conference on Multidisciplinary and Current Technical Research-2023
Technical Program Committee (TPC) of ISCMCTR-2023 is pleased to inform you that your paper [Paper ID: 47, Title: Process-in-Loop Analysis of Universal Control Technique for a Hexagonal-Shaped Reduced Device Multilevel Inverter], has been accepted for presentation in the International Student Conference on Multidisciplinary and Current Technical Research-2023, MITS Gwalior, and provisionally accepted for publication, subjected to:

- Satisfactory revision of paper based on enclosed reviewer comments
- Presentation of paper by one author during the conference on May 20-21,2023
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Reviewer's Comments:
The manuscript "Process-in-Loop Analysis of Universal Control Technique for a Hexagonal-Shaped Reduced Device Multilevel Inverter" is presented in proper way. The presented research work is worthy for acceptance.
Few minor corrections in the manuscripts are as follows-

1. Latest references of years from 2019 to 2023 should be added in the manuscript.
2. In order to provide a research path for the upcoming researchers in the similar field, the future scope of the work may be added in the conclusion.
3. At few places, authors are using the statement "as shown in fig", but they are not writing the figure numbers. All the figures must be the properly cited in the text body.
4. Plagiarism in the manuscript is quite high. Reduce the Pilgrims as per the conference guidelines.

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Addressing comments or suggestions received during the presentation at the conference, if any, and their inclusion in the final paper may also be required before publication.

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