A Project Report

on

Experimental in loop analysis of Reduced Device Count Hybrid Multi-Level Inverter Topology control by Universal Control Technique

in partial fulfillment for the award of the degree

of

BACHELOR OF TECHNOLOGY (B. TECH)

IN

ELECTRICAL ENGINEERING

Submitted by:

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MAY 2023

CANDIDATE'S DECLARATION

I hereby declare that the project titled "**Experimental in loop analysis of Reduced Device Count Hybrid Multi-Level Inverter Topology control by Universal Control Technique**" submitted for the award of **Bachelor of Technology** degree in **Electrical Engineering** is my original work and the project has not been submitted elsewhere for the award of any other degree, diploma, fellowship, or any other similar titles.

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Place: Gwalior

Date:25 May 2023

This is to certify that the above statement made by the candidate is correct to my knowledge and belief.

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ACKNOWLEDGEMENT

I would like to express my sincere appreciation to my supervisor Prof. Praveen Bansal for his guidance, encouragement, and support throughout the course of this work. It was an invaluable learning experience for me to be one of their students. From them I have gained not only extensive knowledge, but also a careful research attitude.

I am also thankful **Prof. Praveen Bansal** for his cooperation with me in facilitating the infrastructure and lab facility during my work.

I am highly indebted to Dr R.K. Pandit, Director M.I.T.S., Gwalior (M.P.) for the facilities provided to accomplish this internship.

I would like to thank Dr S. Wadhwani, Head Department of Electrical Engineering, M.I.T.S., Gwalior (M.P.) for his constructive criticism throughout my internship.

I would like to thank Mr. Vikram Rajput, T&P Coordinator MITS, Gwalior & Prof. Praveen Bansal, Internship Coordinators, Department of Electrical Engineering for their support and advice to get and complete internship in above said organization. I am extremely grateful to my department staff members and friends who helped me in successful completion of this internship.

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ABSTRACT

This research paper explores the hybrid topology of symmetrical nine-level inverter that uses fewer devices and a universal control PWM technique. The objective is to develop an efficient and cost-effective solution for power electronics applications. The proposed hybrid topology combines the advantages of the cascaded H-bridge and flying capacitor topologies to reduce the number of required devices. The universal control PWM technique is used to generate the gating signals for the inverter switches, ensuring reliable and precise control of the output voltage. Simulation and experimental results demonstrate the effectiveness of the proposed hybrid topology and universal control PWM technique in achieving high-quality output voltage waveforms with reduced harmonic distortion and lower switching losses. The proposed approach presents a promising solution for improving the performance and reducing the cost of multilevel inverters (MLI).

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Number

1. PWM- Pulse Width Modulation
2. MLI-Multilevel Inverter
3. FC-Flying Capacitor
4. NPC-Neutral Point Clamped
5. CHB-Cascaded H-Bridge
6. PD-Phase Disposition
7. POD-Phase Opposition Disposition
8. APOD-Alternate Phase Opposition Disposition
9. VFISC-Variable Frequency Inverse Sinusoidal Carrier

CHAPTER I: INTRODUCTION

Recent years have witnessed substantial advancements in the field of power electronics, and multilevel inverters are now a crucial component of contemporary power conversion systems. Due to its capacity to deliver high-voltage output with little harmonic distortion, the multilevel inverter technology is being employed in a growing number of applications, including motor drives, power transmission systems, and renewable energy systems.

The harmonic reduction of an inverter output current in a typical two-level inverter arrangement is done mainly by increasing the switching frequency. However, because of the higher switching losses and the amount of dc-bus voltage in high power applications, the power device's switching frequency must be limited below 1 KHz. On the other hand, the electromagnetic disturbance and motor winding stress are caused by the extremely high dv/dt produced with high dc-link voltage. Multi-level inverters are better from the perspective of distortion reduction and high dc-link voltage level.

MLI does have certain limitations, however, including the need for more peripheral devices like gate driver circuits, protection circuits, and heat sinks as output levels are increased [3]. The total system becomes more complicated, heavy, and expensive as the number of devices increases, which also lowers the converter's efficiency and reliability.

The Reduced Device Topology-MLI is a topology that addresses these issues by using a reduced number of switching devices. The RDT-MLI topology provides several advantages over traditional multilevel inverters, including reduced cost, low switching losses, and the ability to easily expand the system to achieve higher voltage levels [4]. As a result, many topologies and control schemes have been presented in recent years with fewer devices and that use a combination of unidirectional and bidirectional switches with varying ratings.

By changing the width of the pulses sent to each switch, universal control pulse width modulation (UCPWM), a modulation technique, can be used to regulate the inverter's output voltage. In comparison to conventional two-level inverters, utilizing a multi-level inverter with UCPWM may provide advantages such as better power quality, less harmonic distortion, and higher efficiency. Additionally, the use of UCPWM permits greater control over the output voltage, allowing for the optimization of energy efficiency and adaptation to changes in load conditions.

The implementation of a nine-level inverter using the universal control PWM technique is the major subject of our research article. A potential area of research in the realm of power electronics is the application of the universal control PWM approach in a nine-level multilevel inverter. This method is easier to use and less expensive than others since it only needs one controller to produce the pulse width modulation signal for each level of the multilevel inverter.

1.1 Objective

a) Simulating and Analyzing the Circuit: The aim is to study a nine-level multilevel inverter circuit's behavior under different operating situations and to model the circuit using Simulink blocks to examine the output waveforms.

b) Performance Evaluation: The goal is to assess the output waveform quality and total harmonic distortion (THD) of the nine-level multilevel inverter. This would entail examining the simulation results and contrasting them with hardware results.

c) Design Optimization: The purpose is to optimize the nine-level multilevel inverter's architecture in order to accomplish objectives, including minimizing THD, reducing switching losses, or increasing efficiency. This can entail modifying variables like the modulation index and switching frequency and then assessing how the changes affect the system's performance.

d) Comparative Analysis: The goal is to evaluate the nine-level multilevel inverter's performance in comparison to other multilevel inverter topologies. This could entail simulating and examining several topologies under comparable operating settings and contrasting their benefits, drawbacks, and performance traits.

1.2 Problem Formulation

a) Total harmonic distortion (THD) is a significant component of low-level inverters.

b) Low-Level inverter does not provide good quality of output waveforms.

c) In high-power and high-voltage applicants low-level inverter have some limitations in operating at high frequency.

1.3 Solution Methodologies

Implementation of a 9-level inverter to mitigate the drawbacks of low-level inverter use:

a) Increasing the level of inverter will make the resultant waveform move toward the sinusoidal waveform which automatically improves the waveform quality.

b) The proposed topology employs less number of switching devices which reduces the switching losses and also make it cost effective.

c) With minimal overall harmonic distortion, the proposed topology of the multilevel inverter enables high voltage levels.

CHAPTER II: Introduction to Multilevel Inverters: Topologies, Advantages, and Applications.

2.1 Multi-Level Inverters

Due to their capacity to produce high-quality voltage waveforms with reduced harmonic distortion and improved voltage control, multi-level inverters have drawn a lot of attention in recent years. These inverters offer an effective and dependable solution for several applications, including motor drives, power grid systems, renewable energy systems, and inverter systems. They provide benefits over conventional two-level inverters, such as improved voltage resolution, reduced electromagnetic interference (EMI), and lessened stress on power components, by using several levels of voltage.

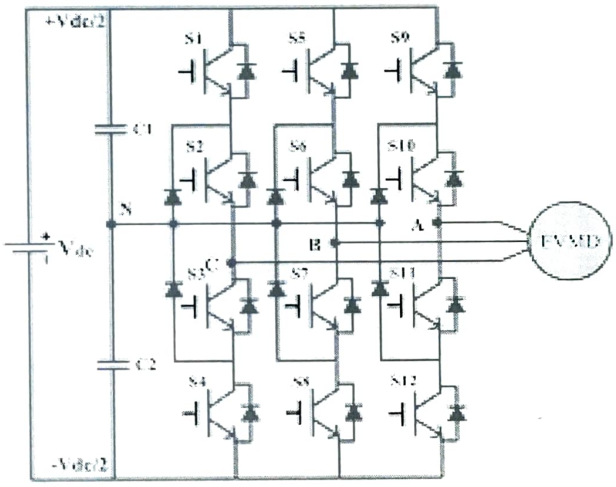


Fig.1.Diode-Clamped Multilevel Inverter

A multi-level inverter's fundamental working theory entails integrating many levels of voltage from various power semiconductor devices to create the required output voltage waveform. To do this, power semiconductor switches are linked in series or parallel to produce various output voltage levels. The creation of near sinusoidal waveforms with lower harmonic content is made possible by the independent regulation of each voltage level.

2.2 Advantages of Multi-Level Inverter

a) High Power Quality.
b) Produce High Voltage.
c) Less Filter Requirement.
d) Low Switching Losses.
e) Enhanced Staircase Waveform Quality.
f) Electromagnetic Interferences reduces.
g) Generate less common-mode Voltages.
h) dv/dt stress gets reduced on the switching devices.
i) Can modulated with both fundamental frequency and high frequency switching scheme.

2.3 Multilevel Inverter Topologies

2.3.1 Flying Capacitor (FC) Multilevel Inverter

A type of a multilevel inverter that use flying capacitors to create stepped voltage waveforms is the flying capacitor multilevel inverter. The output of a flying capacitor inverter exhibits a stepped voltage waveform because each phase is connected to a group of capacitors that are switched between the load and the DC supply.

A flying capacitor multilevel inverter's key benefit is that it can provide an output waveform of excellent quality and low harmonic distortion, which is crucial for applications like motor drives and renewable energy systems. The biggest drawback is that it necessitates a lot of capacitors, which might raise the system's cost and complexity.

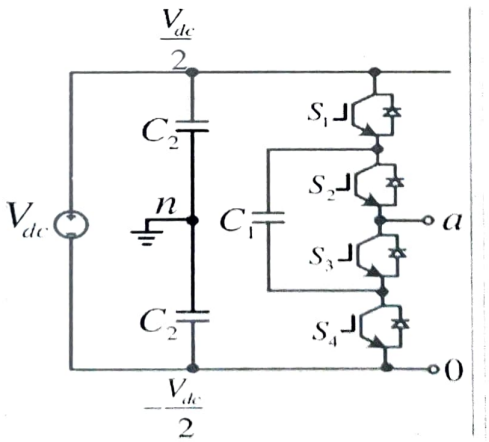


Fig.2. Flying Capacitor Multilevel Inverter

2.3.2 Diode Clamped Multilevel Inverter

It is also referred to as an "NPC inverter" or "neutral point clamped inverter." An inverter that uses clamping diodes to limit the voltage across each of its phases is known as a diode-clamped inverter. The output waveform can then be controlled more precisely by generating numerous voltage levels that are higher than the input DC voltage.

The diode-clamped inverter's advantage is its capacity to generate high-quality output with minimal harmonic distortion. The diode-clamped inverter's drawback is that it requires more parts and is more complicated than other inverter kinds. To ensure effective operation and fault protection, it also needs careful design as well as control.

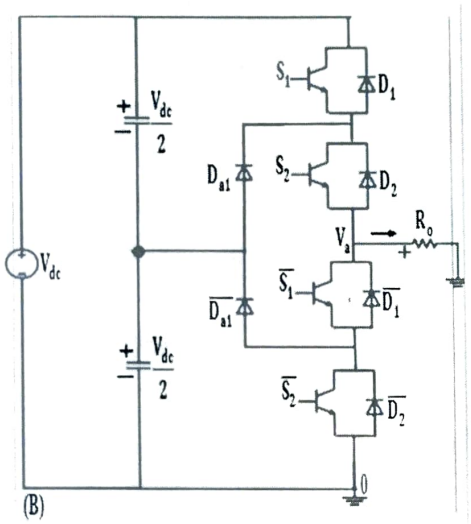


Fig.3.Diode Clamped Multilevel Inverter

2.3.3 Cascaded H-Bridge (CHB) Multilevel Inverter

Several H-bridge inverter units are connected in series to create a cascaded H-bridge multi-level inverter, which creates a multi-level output voltage waveform. Usually, four power switches, such as MOSFETs or IGBTs, are assembled into an H-bridge unit, which is then placed in a bridge configuration.

Cascaded H-bridge inverters have the benefit of producing a high-quality output voltage with minimal harmonic distortion, which makes them appropriate for use in applications requiring a high-quality AC power supply.

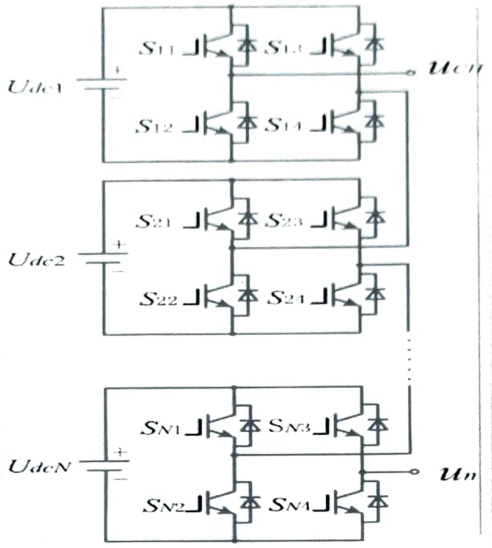


Fig.4. Cascaded H-Bridge Multilevel Inverter

2.4 Proposed Topology

Fig.5. depicts the topology configuration. The voltage divider circuit is made up of two DC voltage sources, V and 2V. The controlled switch IG7, along with the four diodes D1, D2, D3, and D14, constitute an auxiliary switch that is connected to the HSC, which is made up of six switches IG1, IG2, IG3, IG4, IG5, and IG6. It can be referred to as symmetrical MLI if the levels of the DC voltage sources are equivalent.

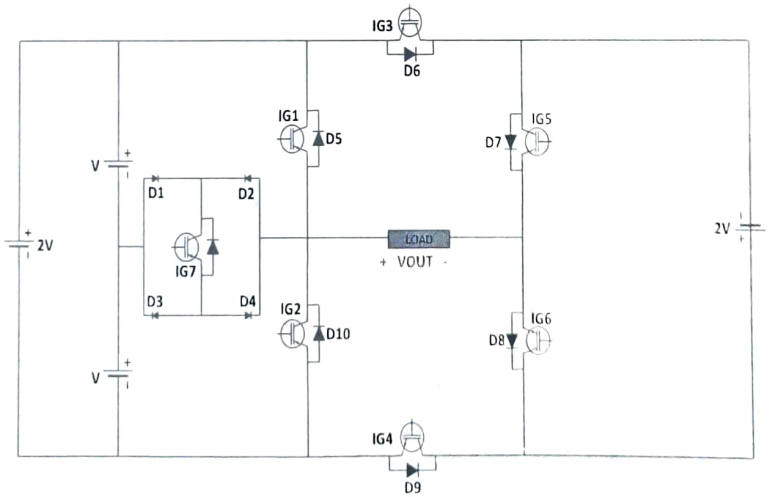
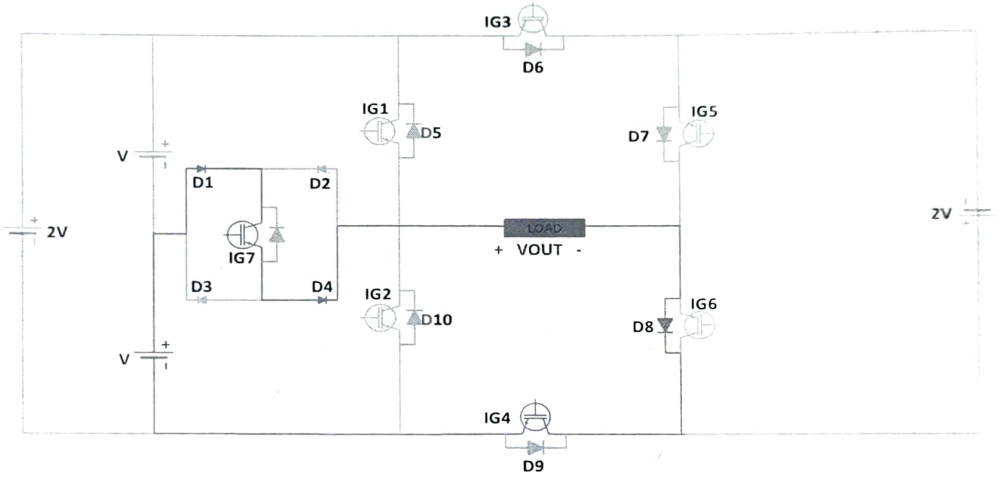


Fig.5. Basic Structure of proposed Topology

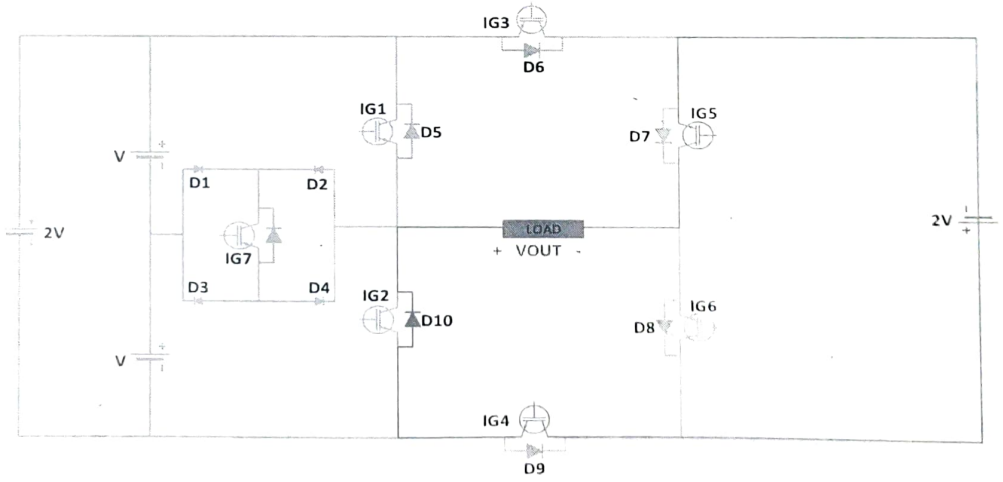
Main power switches: The proposed topology-I in symmetrical configuration reduces the number of main power switches needed by 56.25% (7 instead of 16) as compared to classical topologies.

Power diodes: The suggested topology-I in symmetrical arrangement reduces the number of power diodes needed by 37.5% (10 instead of 16) when compared to Flying Capacitor and Cascaded H-Bridge, and by 86.11% (10 instead of 72) when compared to Neutral Point Clamped.

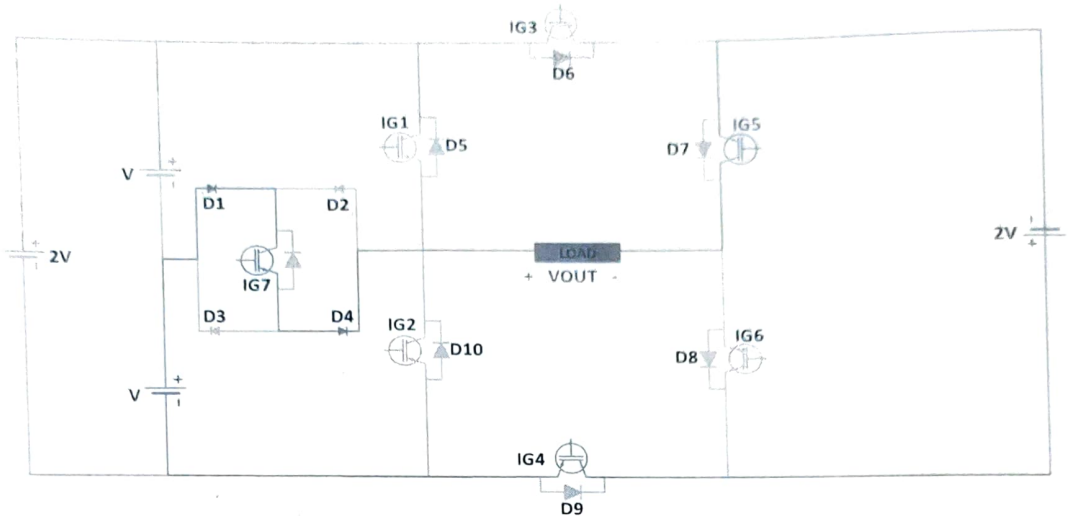
Fig. 6. demonstrates the different levels obtained using different switching modes



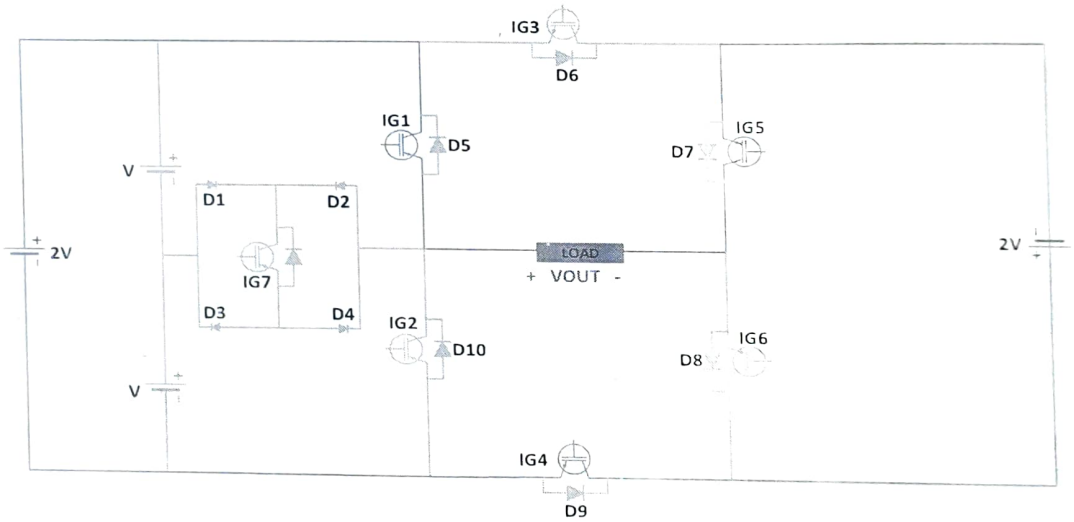
a) **Stage 1**



b) **Stage 2**



c) **Stage 3**



d) **Stage 4**

Fig.6. Level generation procedures of output voltage: (a) 1V; (b) 2V; (c)3V; (d)4V.

Table 1 summaries each switching configuration that was employed to produce the necessary output of Nine- level.

Table 1 Switching configuration

For Positive Cycle

Output levels, V	ON State Switches	Conducting Diodes
1	IG4, IG7	D1, D4, D8
2	IG4, IG5	D10
3	IG4, IG5, IG7	D1, D4
4	IG1, IG4, IG5	----------.

For Negative Cycle

Output levels, V	ON State Switches	Conducting Diodes
-1	IG3, IG7	D2, D3, D7
-2	IG3, IG6	D5
-3	IG3, IG6, IG7	D2, D3
-4	IG2, IG3, IG6	---------

2.5 Comparison of Various Symmetrical Nine-Level Inverter Topologies

There are various advantages of using proposed topology based inverter instead of using the traditional Multi-Level inverter.The biggest advantages is that it requires less number of devices which effectively reduce the cost of inverter as well as the switching losses and hence efficiency also increases .Table 2 compares the proposed topology inverter with three widely used traditional multi-level inveters on the basis of number of devices used in it.

Table 2 Evaluation Of Different Symmetric Nine-Level Inverter Topologies

ELEMENTS	NPC	FC	CHB	PROPOSED TOPOLOGY
Main Power Switches	16	16	16	6
Auxiliary Switch	0	0	0	1
Diodes	72	16	16	10

2.6 Application

a. Static VAR Compensation.
b. Variable Speed Motor Drives.
c. High Voltage System Interconnections.
d. High Voltage AC and DC Transmission Lines.

CHAPTER III: Adaptive Control and Modulation Techniques: Towards Universal Scheme Design

This chapter examines the importance that adaptive control and modulation techniques play in the creation of universal control systems. It talks about the idea of adaptivity in control systems and how it makes it possible to modify control settings in response to real-time circumstances. The chapter explores several adaptive control systems in more detail and highlights how they can be integrated with modulation techniques to achieve reliable and effective control across a variety of domains.

3.1 Universal Control Scheme

In this section, the suggested universal control technique is explained. It can be used with any multilevel inverter topology because of the way it is designed. Let the total number of levels in the phase voltage for the supplied inverter will be N level. If N level is greater than 3, a voltage source inverter can function at various levels. Since level 0 is noteworthy, level N is viewed as odd. The N level waveform's number of positive levels will also be:

$$N = (N_{level} - 1)/2$$

A sinusoidal waveform of amplitude Bref and frequency f_{ref} constitutes the modulating signal $b_{ref}(t)$. For sine PWM and low-frequency schemes, there needs to be triangular, constant, 2N carrier signals. The frequency of these carriers is $fcar$, and Bcar is their peak-to-peak amplitude. Carrier signals that are higher than the zero level are known as $b^{+}_{car,j}(t)$ and those that fall below the zero level are known as $b^{-}_{car,j}(t)$, (j = 1 to N). The zero reference is positioned in the middle of the continuous bands that the carrier signals occupy.

Accordingly, the following quantities can be defined:

Index of frequency modulation, $\boldsymbol{Q = Bcar/\,(Bref)}$

"Q" determines the output waveform's harmonic profile as well as the power switches' switching frequency.

Index of amplitude modulation, $\boldsymbol{L = Bref/\,(NBcar)}$

The output waveform's peak value and number of levels are determined by the value of "L".

Every time, the modulating signal is compared to each carrier. For each comparison, the outcome is either "1" if the modulated signal exceeds the carrier, or "0" otherwise. All carrier signals above the zero reference are affected by this. For each comparison, the outcome is either "0" if the modulating signal exceeds the carrier or "-1" if the carrier signal falls short of the zero reference.

That is.

$$b^{+}_{out,j}(t) = 1, \qquad for\ b_{ref} \geq b^{+}_{car,j}(t)$$

$$=0, \qquad otherwise$$

$$b^{-}_{out,j}(t) = 0, \qquad for\ b_{ref} \geq b^{-}_{car,j}(t)$$

$$= -1, for\ otherwise$$

The results so obtained are combined to create an "Aggregated signal" that is designated as $\boldsymbol{b_{bgg}(t)}$.

That is,

$$b_{bgg}(t) = \sum_{j=1}^{N} (b^{+}_{out,j}(t) + b^{-}_{out,j}(t))$$

It should be observed that the waveshape of $b_{bgg}(t)$ gains the same property as the anticipated output voltage. With a certain topology, power electronic switches require real-world driving signals, which requires the use of logical components and a look-up table to be generated from $b_{bgg}(t)$. Using Boolean operations,

$$b_{d,t}(t)\ are\ derived\ from\ b_{bgg}(t)\ using\ following\ criteria:$$

$$b_{d,t}(t) = 1, if\ b_{bgg}(t) = j$$

$$=$$

$$0, otherwise;\ where, j = -N\ to\ +N$$

As a result, a total of N-level derived signals will be produced, each of which will be used to operate the switches that must remain ON at the voltage level indicated by the output waveform. In order to acquire the switching function $b_{switching}(t)$ for a certain switch, the necessary derived signals would be sent into an OR gate. The mathematical formulation of the switching function is

$$b_{switching}(t) = \overline{\prod \overline{b_d(t)}}$$

Where,

$$\overline{b_d(t)} = 1 - b_d(t)$$

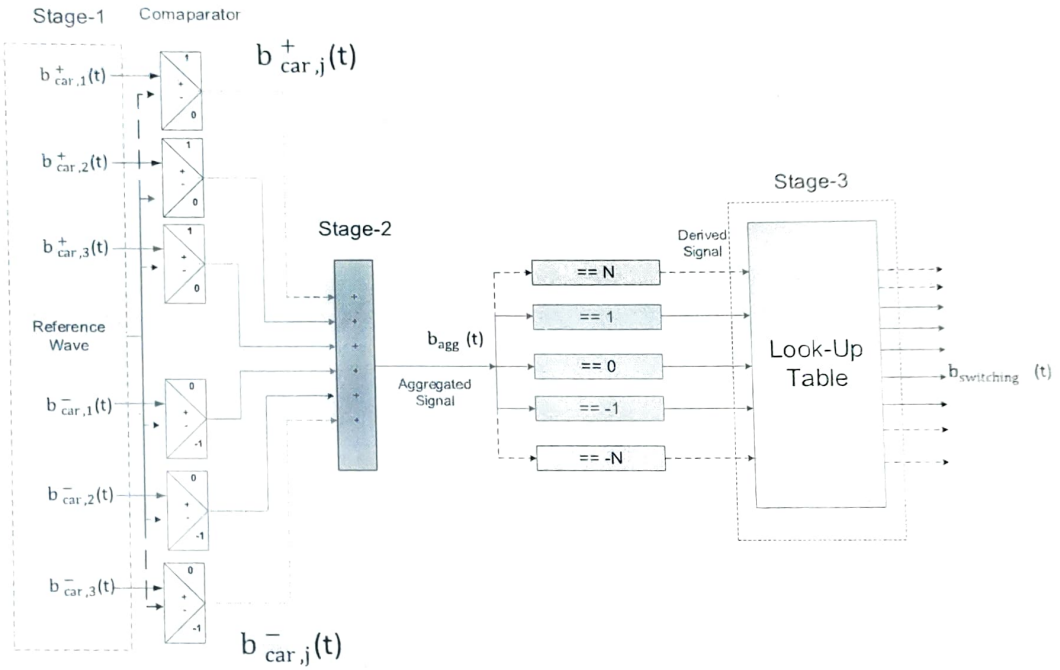


Fig.7. Block Diagram of Universal Control Scheme

3.2 Control and Modulation Techniques in Proposed Topology

In the literature, several modulation techniques for MLIs have been suggested. The many carriers used in multilevel carrier-based PWM techniques can be triangular or saw-tooth signals. Frequency, phase of each carrier, amplitude, and offset between the carriers are all variables that are free in carrier signals. Additionally, the reference wave (modulating signal) offers flexibility in terms of frequency, amplitude, and phase angle, as well as the injection of zero sequence signals. As a result, a variety of multilevel carriers-based PWM techniques can be obtained by using these combinations. An inverter with n levels of phase voltage would typically need a series of n -1 carrier signals. These Modulation Techniques are as:

3.2.1 Phase Disposition PWM

An inverter's output voltage can be regulated using a phase disposition technique, a form of modulation technique, in power electronics. The outcome is a stepped output waveform, which is achieved by segmenting the input voltage waveform into various parts and applying various voltage levels to each part. This method is appropriate for high power applications such as motor drives and renewable energy systems since it can produce more output voltage levels than conventional two-level inverters.

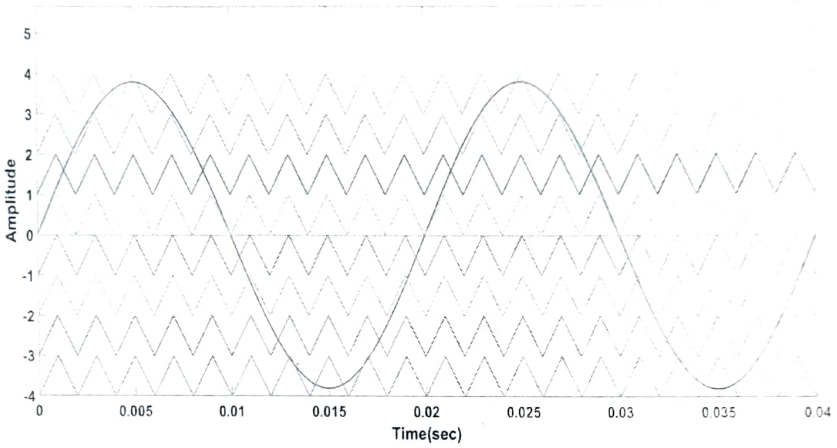


Fig.8. PDPWM

3.2.2 Phase Opposition Disposition (PODPWM) PWM

A modulation technique called phase opposition disposition (POD) is used in power electronics to regulate an inverter's output voltage. In order to produce a stepped output waveform, it first generates two sets of output voltage waveforms with opposite polarities.

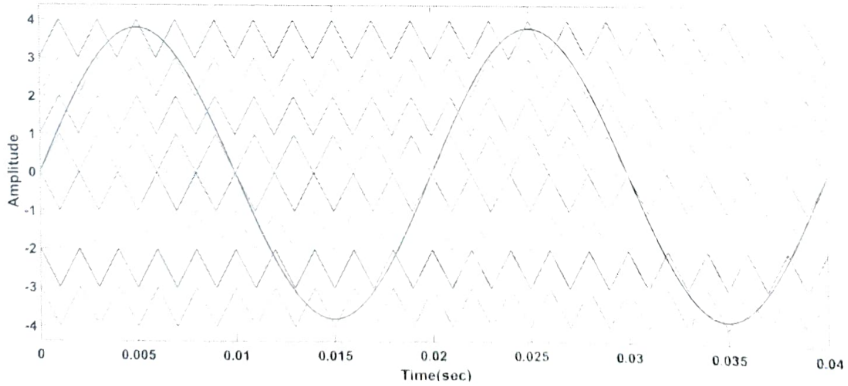


Fig.9. PODPWM

3.2.3 Alternate Phase Opposition Disposition (APODPWM) PWM

Alternate Phase opposition disposition (APOD) is a modulation method used in power electronics to regulate the inverter's output voltage. In this approach, the carrier signals alternatively phase-displace by 180 degrees.

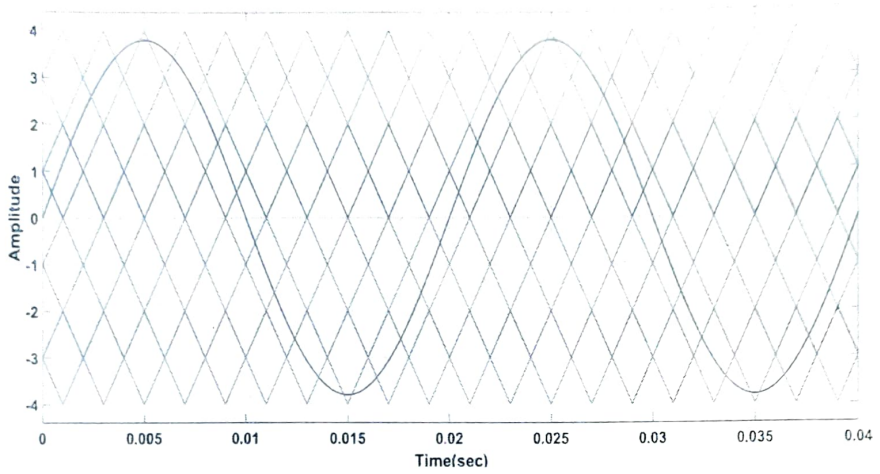


Fig.10. APODPWM

3.2.4 Variable Frequency Inverse Sinusoidal Carrier PWM(VFISCPWM)

This method uses an inverted sine wave with variable frequency as the carrier wave and a sine wave as the reference wave, with the carrier signals having different frequencies from one another. The control technique will produce pulses whenever the reference sine wave's amplitude exceeds that of the inverted sine carrier wave.

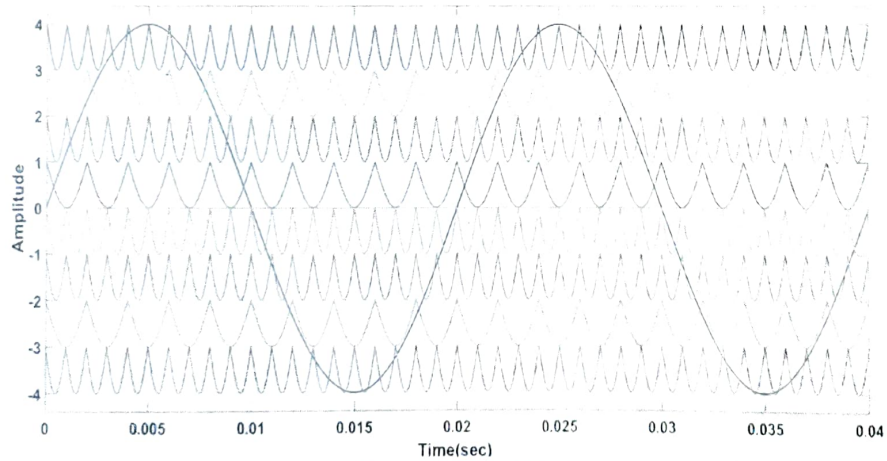


Fig.11. VFISCPWM

3.2.5 Inverted Sinusoidal Carrier PWM

In this method, a sine wave serves as the carrier wave. The inverted sine carrier PWM (ISCPWM) technique uses an inverted sine carrier with a high frequency as the carrier signal and a sine wave as the reference signal. Low harmonic distortion is achieved by combining reference and carrier signals with different modulation indices.

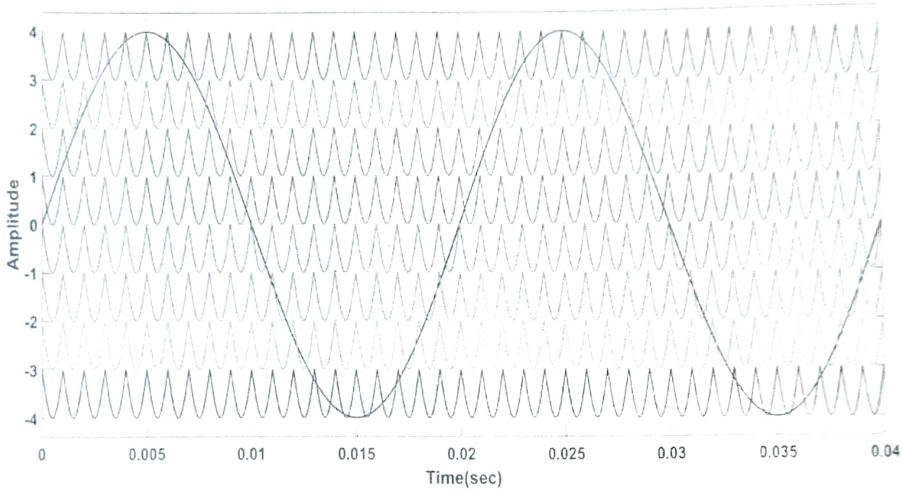


Fig.12. ISCPWM

CHAPTER IV: RESULTS AND DISCUSSION

The purpose of this chapter is to describe and evaluate the findings of a research study on a nine-level multilevel inverter. The chapter includes a summary of the experimental setup, including the inverter's specs and the testing procedures used.

The chapter then moves on to provide the results, emphasizing the nine-level multilevel inverter's major performance indicators and traits. This comprises elements like the waveform of the output voltage and the total harmonic distortion (THD).

4.1 Simulation Results

Using MATLAB/SIMULINK R2016a, the suggested multilevel inverter topology is simulated. The following simulation parameters are R=50 ohms and V=12 volt for dc voltage. The switches are considered to be perfect, and the carrier signal frequency in this paper's five PWM approaches is 10 kHz. These techniques include PD, POD, APOD, ISC, and VFISC, each with a distinct Modulation Index (MI). In table 3, the THD of five PWM techniques are displayed. In MATLAB/Simulink, the harmonic spectrum is calculated via FFT analysis.

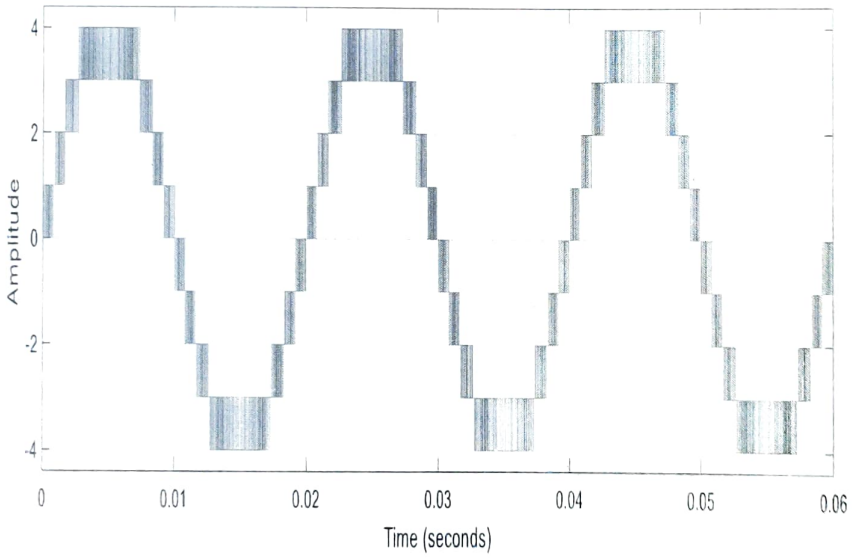


Fig.13. Output Waveform of Proposed Topology

4.2 FFT Analysis of Different Techniques

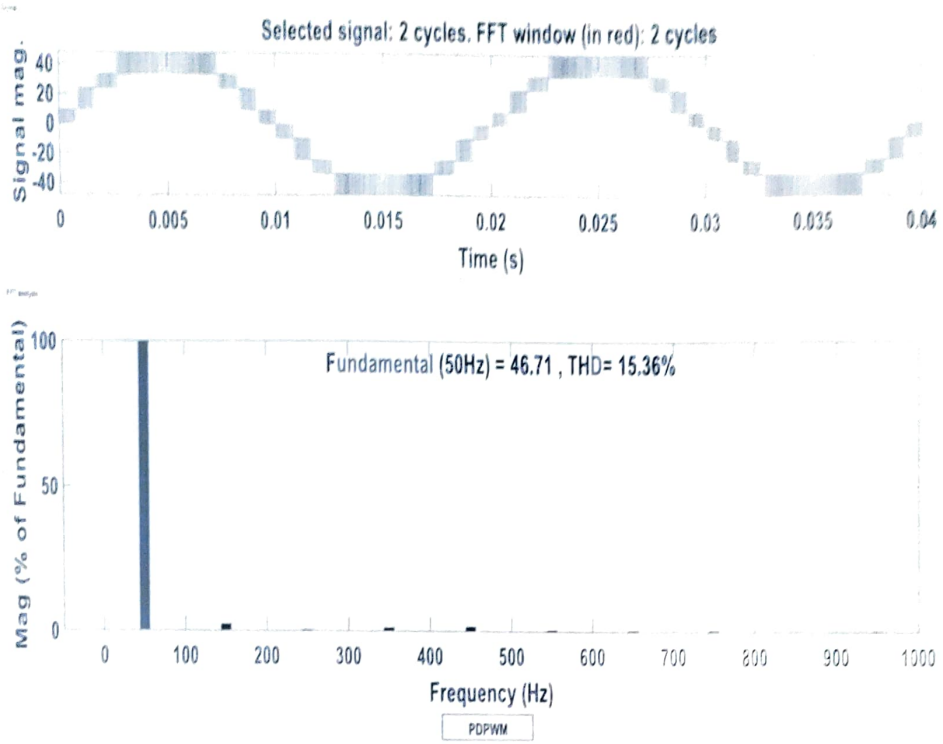


Fig.14. THD in 9-level inverter with PDPWM Technique

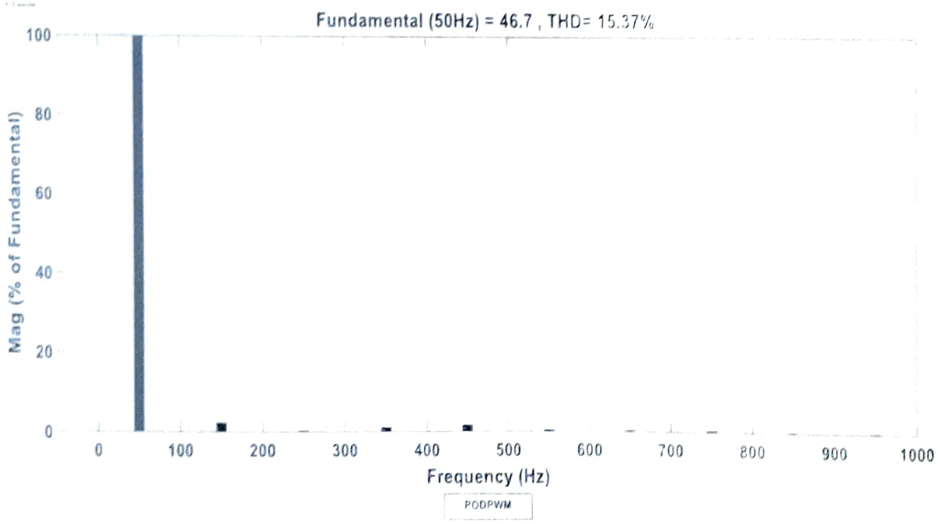


Fig.15. THD in PODPWM Technique

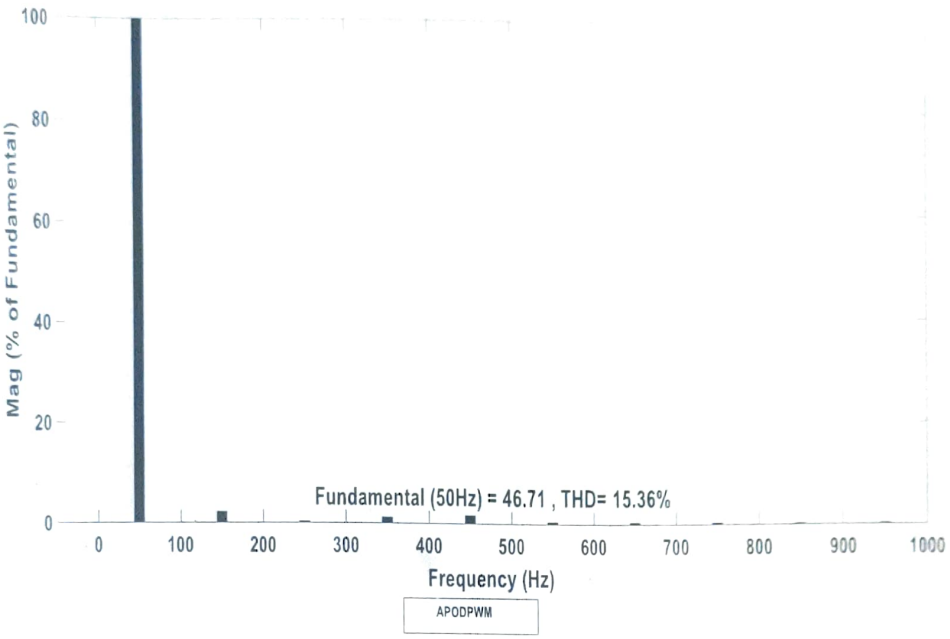


Fig.16. THD in APODPWM Technique

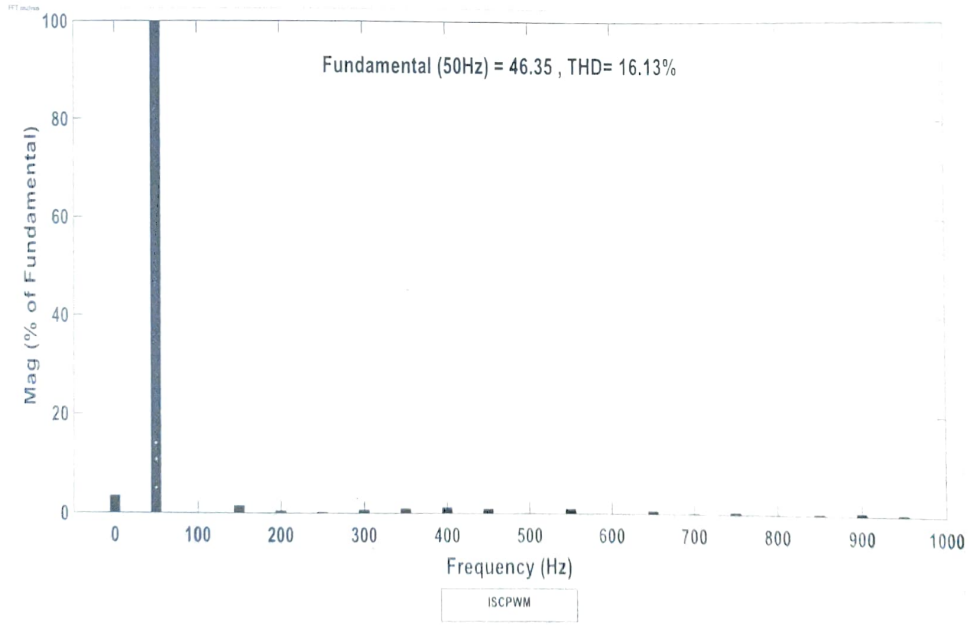


Fig.17. THD in ISCPWM Technique

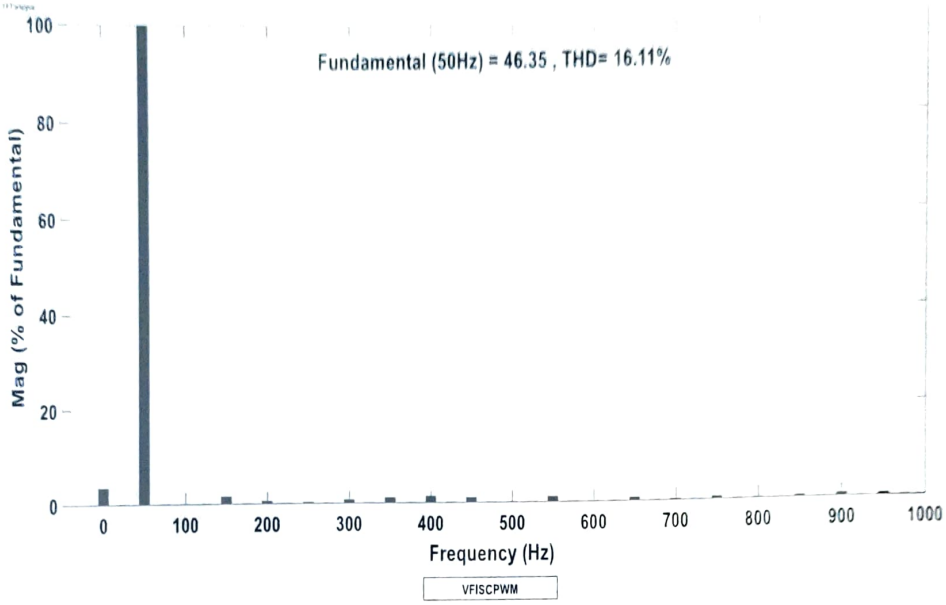


Fig.18. THD in VFISCPWM Technique

Table 3 Results of different modulation technique

Level	Modulation Index	Modulation Technique				
		PD	POD	APOD	VFISC	ISC
9-level	1.1	14.31	14.30	14.30	14.96	14.94
	1.0	15.36	15.37	15.36	16.11	16.13
	0.9	16.78	16.71	16.71	17.72	17.72
	0.8	18.23	17.71	17.72	18.03	18.02

4.3 Experimental Results and Discussions

In the paper, the universal control techniques have been implemented to control the MLI. Six different PWM modulations techniques have been presented on varying modulation index. In experimentation, a low cost STM32F4 discovery board haven been used to verify universal technique experimentally. The experimental photograph is shown in Fig.19. The discovery board has ARM Cortex-M4 32-bit microcontrollers installed and have fifteen analog to digital pin (PA0-PA7, PB0-PB1 and PC0 to PC5) , two digital to analog pins (PD0-PD1),. In this paper DAC pins are used to extract the outputs of multilevel inverter. Real-time implementation of created Simulink models can be readily created and loaded into the board memory by using Keil, STM32F4 embedded coder target, together with other useful tools.

Create a model using Simulink that includes embedded target blocks in accordance with the applications and accessibility requirements. Before creating any files for Simulink models, ensure that the primary directory path is correctly located in MATLAB's command window. Simulink models can be created and executed on a discovery kit by using the Support packages for STMicroelectronics' STM32F4 exploration board. Integrated into the support package are Simulink blocks for setting and gaining access to board's auxiliary devices. The STM32F4 blocks' third-party interface, in addition to MATLAB, is Waijung software. The user must install the STM link utility driver before they can finish installing the Waijung block. Choose the parameters for the target arrangement based on your requirements. Fig.16-18 displays the experimental findings at various modulation indices.

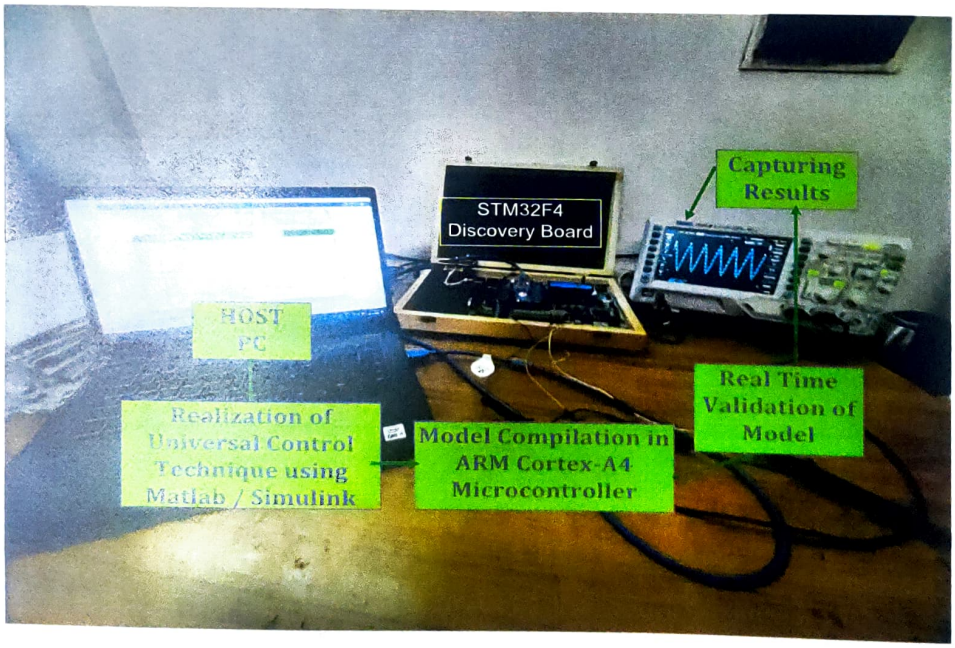


Fig.19. Experimental Realization of Universal Control Technique

Fig.20. Experimental Output Voltage at modulation index of 1

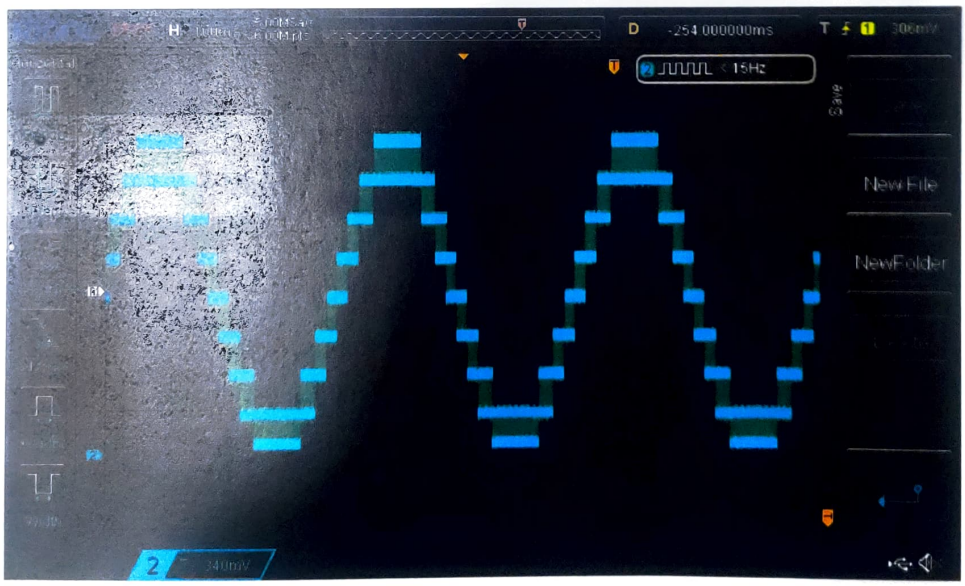


Fig.21. Experimental Output Voltage at modulation index of 0.9

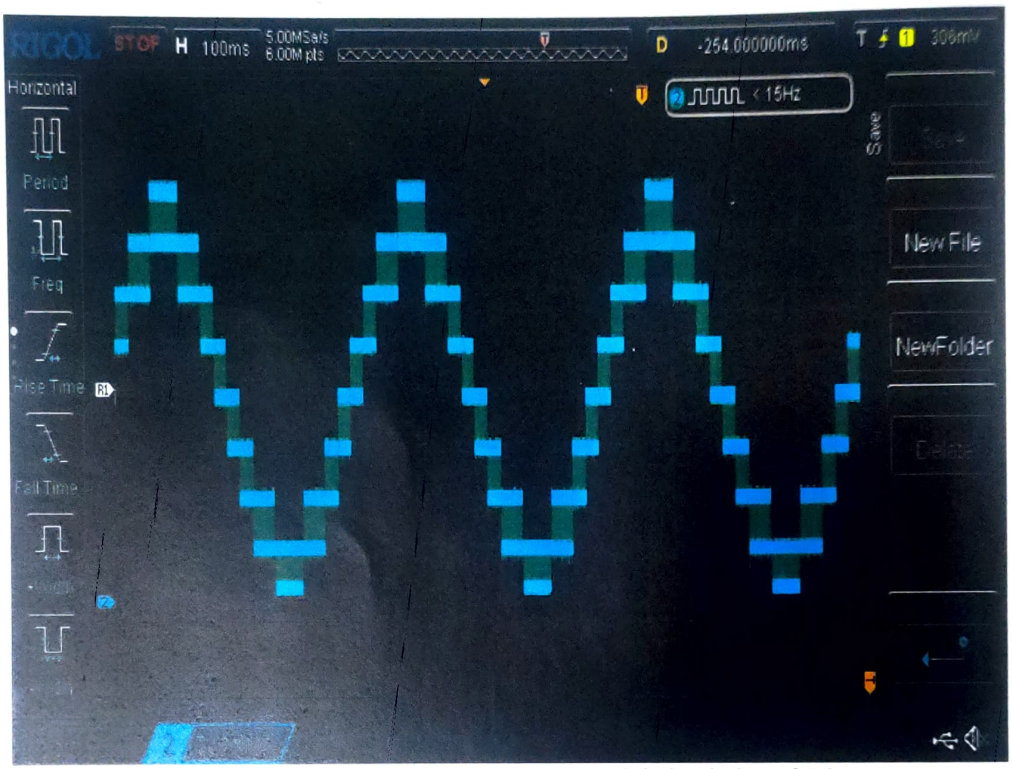


Fig.22. Experimental Output Voltage at modulation index of 0.8

CHAPTER V: CONCLUSION

In place of the traditional multilevel inverters, a new nine-level inverter design was introduced in this study for the grid-integrated system. The number of components was decreased by the suggested topology. Moreover, it ensures the lowest hardware implementation cost. The suggested inverter topology is controlled by switching pulses produced by the low-frequency modulation approach, which also offers the lowest total harmonic distortion. There is no need for a filter with the suggested inverter. Consequently, in the future power system, the proposed inverter topology makes the grid-connected systems more compact, efficient, and dependable. The simulation outcomes for an inverter with a 9-level design have been given. It was shown that the inverter's THD varies when different PWM techniques are applied, and the Phase Opposition Disposition (POD) Method achieves the lowest THD.

BIBLIOGRAPHY

[1] Baker, R.H., Bannister, L.H.: 'Electric power converter', US Patent 3 867 643, February 1975.

[2] G Singh. and V.K. Garg, "THD analysis of Cascaded H-Bridge Multi-Level Inverter," 2017 4th International Conference on Signal Processing , Computing and Control (ISPCC), pp. 1-6.

[3] M. Shamil, M. Darwish and C. Marouchos, "Single phase Multi level inverter with desire harmonics," 2012 47th International Universities Power Engineering Conference (UPEC), London, 2012, pp. 1-4.

[4] K. K. Gupta and S. Jain, "A novel universal control scheme for multilevel inverters," 6thIET International Conference on Power Electronics, Machines and Drives (PEMD 2012), Bristol, 2012, pp. 1-6.

[5] OUnejjar, Y; Al-Haddad, K; Gregoire, L; , "Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation," Industrial Electronics, IEEE Transactions on , vol.58 ,no. 4, pp. 1294-1306, April 2011.

[6] N. Prabaharan and K. Palanisamy, "A new hybrid asymmetric multilevel inverter with reduced number of switches", *2016 IEEE International Conference on Power Electronics Drives and Energy Systems (PEDES)*, pp. 1-4, 2016.

[7] Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., Sabahi, M.: 'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels', IET Power Electron., 2014, 7, (1), pp. 96–104.

[8] Arif, MSB, Sarwer, Z, Siddique, MD, Md. Ayob, S, Iqbal, A, Mekhilef, S. Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. Int J Circ Theor Appl. 2021; 49: 1757– 1775. https://doi.org/10.1002/cta.2971.

[9] Malinowski, M., Gopakumar, K., Rodriguez,J., and Perez, M.A., "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol.57, no.7, pp.2197-2206, Jul.2010.

[10] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point clamped PWM inverter", *IEEE Trans. Ind. Applicat.*, vol. IA-17, pp. 518-523, Sept./Oct. 1981.

[11] A. Kumar and P. Bansal, "A novel symmetrical multilevel inverter topology with reduced switching devices using different PWM techniques", *International Conference on Electrical*

Electronics Signals Communication and Optimization (EESCO'15), pp. 1-6. 24–25 January 2015.

[12] Jani Rushiraj and P.N. Kapil, "Analysis of Different Modulation techniques for multilevel inverters," in ISTIEEE International conference on power electronics, Intelligent control and energy system, 2016.

[13] Agrawal N, Tomar SS, Bansal P (2017)A multilevel inverter topology using reverse-connected voltage sources. In 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), Chennai, 2017, pp 1290–1295.

[14] Nikhil Agrawal and P. bansal, "A new 21-level Asymmetrical multilevel inverter topology with different PWM techniques", *IEEE Conference RDCAPE 2017*, pp. 224-229.

[15] P. Omer, J. Kumar and B. S. Surjan, "A New Multilevel Inverter Topology with Reduced Switch Count and Device Stress," 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur, India, 2018, pp. 1-6.

[16] A. Habib, M. A. Alam, M. T. Islam, M. F. Rahman, A. Mimi Raka and M. R. Awal, "A Novel Asymmetric Nine Level Inverter with Reduced Device Count Suitable for Renewable Energy Applications," 2022 4th International Conference on Sustainable Technologies for Industry 4.0 (STI), Dhaka, Bangladesh, 2022, pp1-6.

[17] S. K. Ghanapuram, D. Sirimalla, V. Edla, S. K. Bykani and L. Utpalla, "Reduced Device Count 9-Level Inverter for Standalone Applications," 2023 7th International Conference on Computing Methodologies and Communication (ICCMC), Erode, India, 2023, pp. 1422-1

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