A Project Report

On

"Experimental Realization of Universal Control Scheme for Asymmetrical Reduced Device Count Multilevel Inverter"

In partial fulfillment for the award of the degree

Of

BACHELOR OF TECHNOLOGY (B. TECH)

IN

ELECTRICAL ENGINEERING

Submitted By:

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(A Govt. Aided UGC Autonomous & NAAC Accredited Institute, Affiliated to RGPV Bhopal)

MAY 2023

CANDIDATE'S DECLARATION

I hereby declare that the project titled **"Experimental Realization of Universal Control Scheme for Asymmetrical Reduced Device Count Multilevel Inverter"** submitted for the award of **Bachelor of Technology** degree in **Electrical Engineering** is my original work and the project has not been submitted elsewhere for the award of any other degree, diploma, fellowship, or any other similar titles.

Kushagra Sharma (0901EE191062)

Place: Gwalior

Date: 25 May, 2023

This is to certify that the above statement made by the candidate is correct to my knowledge and belief.

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ACKNOWLEDGEMENT

I would like to express my sincere appreciation to my supervisor. Prof. Praveen Bansal for his guidance, encouragement, and support throughout the course of this work. It was an invaluable learning experience for me to be one of their students. From them I have gained not only extensive knowledge, but also a careful research attitude.

I am also thankful to my colleagues for his cooperation with me in facilitating the infrastructure and lab facility during my work.

I am highly indebted to Dr R.K. Pandit, Director M.I.T.S., Gwalior (M.P.) for the facilities provided to accomplish this internship.

I would like to thank Dr S. Wadhwani, Head Department of Electrical Engineering, M.I.T.S., Gwalior (M.P.) for his constructive criticism throughout my internship.

I would like to thank Mr. Vikram Rajput, T&P Coordinator MITS, Gwalior & Prof. Praveen Bansal, Internship Coordinators, and Department of Electrical Engineering for their support and advice to get and complete internship in above said organization. I am extremely grateful to my department staff members and friends who helped me in successful completion of this internship.

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ABSTRACT

This paper presents a universal control pulse width modulation (PWM) technique for a single-phase reduced device count Multilevel Inverter. The basic module can produce fifteen level outputs with four dc sources and ten switches. The proposed topology features lower total standing voltage, lower rating switches, and an inherent capacity for producing negative voltage levels.

Harmonics and total harmonic distortion are drawbacks of conventional inverters (THD). This paper uses MATLAB simulation to study the analysis of THD and harmonics. The universal control scheme is tested experimentally using STM32F4 discovery board and a proposed MLI configuration has been tested using various PWM techniques.

Through rigorous experimental testing of the circuit in the lab, the reliability of the simulation results is confirmed.

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Abbreviations

1. MLI – Multilevel Inverter
2. PWM- Pulse Width Modulation
3. THD- Total Harmonic Distortion
4. RDC-Reduced Device Count
5. TSV-Total Standing Voltage

CHAPTER-I
INTRODUCTION

An inverter is a power electronic instrument that transforms dc power into ac power at a specified output voltage and frequency. Two level inverters are inverters that produce an output voltage or current with two distinct values of voltage levels.

The harmonic reduction of an inverter output current in a typical two-level inverter arrangement is done mainly by increasing the switching frequency. However, because of the higher switching losses and the amount of dc-bus volt-age in high power applications, the power device's switching frequency must be limited below 1 KHz. On the other hand, the electromagnetic disturbance and motor winding stress are caused by the extremely high dv/dt produced with high dc-link voltage. Multi-level inverters are better from the perspective of distortion reduction and high dc-link voltage level.

The three-level inverter introduced by Nabae et al. is where the term "multilevel" first appears. The output voltages have more steps when the inverter's level count is increased, creating a staircase waveform with less harmonic distortion. Unfortunately, a large number of levels makes the control complex and causes issues with voltage imbalance.

Multilevel inverters have been widely used in high power applications due to their ability to provide high quality output waveforms with low harmonic distortion. The Reduced Device Topology-MLI is a topology that addresses these issues by using a reduced number of switching devices. The RDT-MLI topology provides several advantages over traditional multilevel inverters,

including reduced cost, low switching losses, and the ability to easily expand the system to achieve higher voltage levels.

1.1 Objective

a) Simulating and Analyzing the Circuit: The aim is to study a nine-level multilevel inverter circuit's behavior under different operating situations and to model the circuit using Simulink blocks to examine the output waveforms.

b) Performance Evaluation: The goal is to assess the output waveform quality and total harmonic distortion (THD) of the nine-level multilevel inverter. This would entail examining the simulation results and contrasting them with hardware results.

c) Design Optimization: The purpose is to optimize the nine-level multilevel inverter's architecture in order to accomplish objectives, including minimizing THD, reducing switching losses, or increasing efficiency. This can entail modifying variables like the modulation index and switching frequency and then assessing how the changes affect the system's performance.

d) Comparative Analysis: The goal is to evaluate the nine-level multilevel inverter's performance in comparison to other multilevel inverter topologies. This could entail simulating and examining several topologies under comparable operating settings and contrasting their benefits, drawbacks, and performance traits.

1.2 Problem Formulation

1. In high-power and high-voltage applicants low-level (for eg. three, five, seven) inverter have some limitations in operating at high frequency.
2. Total harmonic distortion (THD) is a significant component of low-level inverters.

3. Low-level inverter doesn’t provide good quality of output waveforms.

1.3 Solution Methodologies

Implementation of a 15-level inverter to mitigate the drawbacks of low-level inverter use:

1. Increasing the level of inverter will make the resultant waveform move toward the sinusoidal waveform. Increasing the waveform quality.
2. With minimal overall harmonic distortion and no need for a transformer, the proposed Topology of the multilevel inverter enables high voltage levels.
3. The proposed topology employs less number of DC voltage source to produce high level voltages and less number of switching devices which also reduces the switching losses.

1.4 Pulse Width Modulation

Power-electronic switches used in inverters allow for various switching operations to be performed within the inverter to optimize the harmonics and manage the output voltage. A circuit's average output voltage can be altered by varying the pulse width. The name of this method is pulse width modulation.

PWM consists of reference wave (sinusoidal signal) and a carrier wave (triangular signal) and compare them using comparator and producing triggering signals for power-electronics switches. The carrier signals present freedom in the following parameters: frequency, amplitude, phase of each carrier, and offset between the carriers.

In general, an inverter with n_{level} number of levels (including zero level) in the phase voltage, would require a set of n_{level} -1 number of carrier signals.

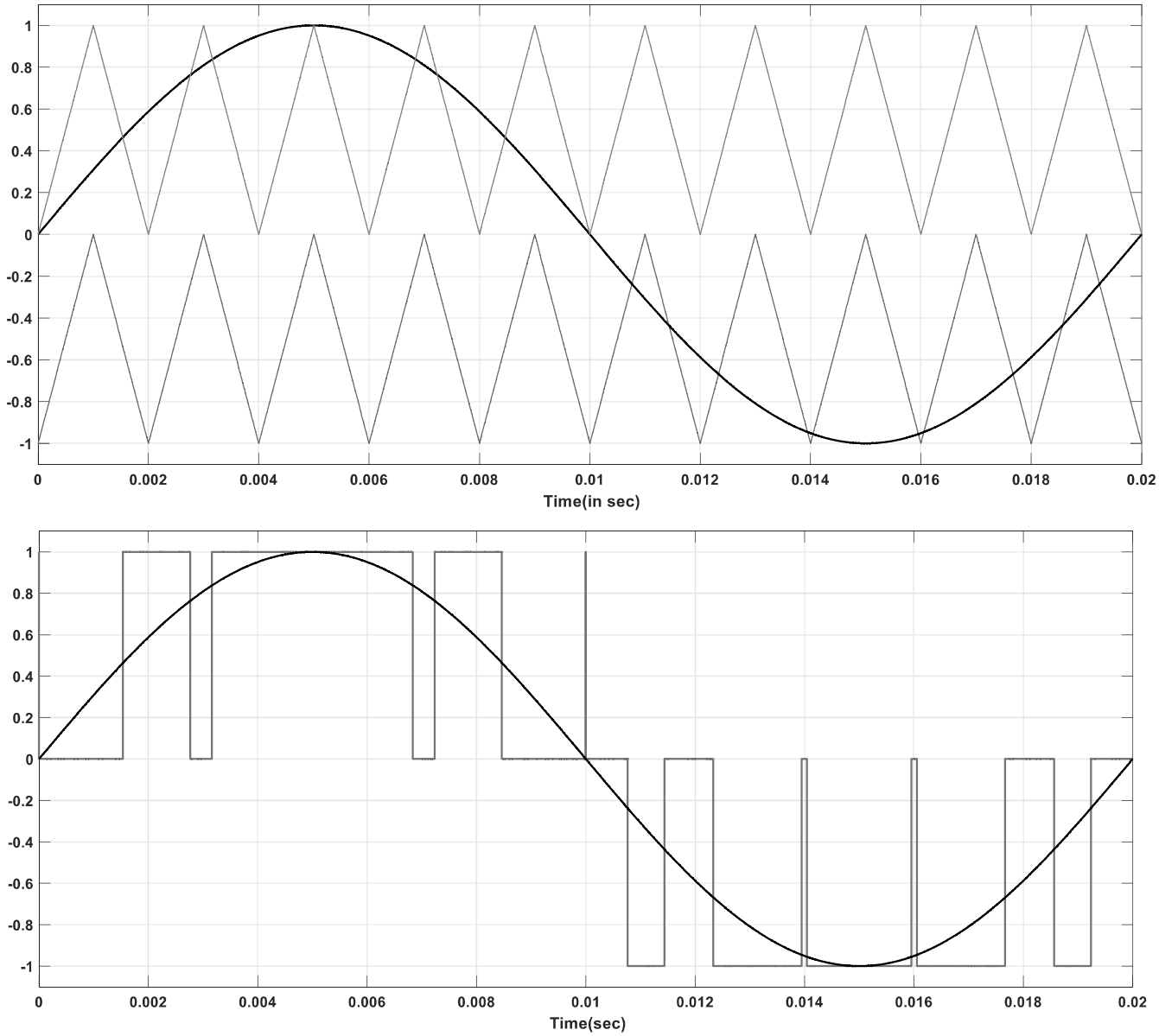


Fig.1 Pulse Width Modulation

CHAPTER II

2.1 INVERTER

The term "inverter" is frequently used to describe a DC to AC converter. This chapter uses the H-bridge inverter or topology as an example. Fig. 2 illustrates a DC source as a battery with voltage VDC. The DC link voltage is a typical term for this output.

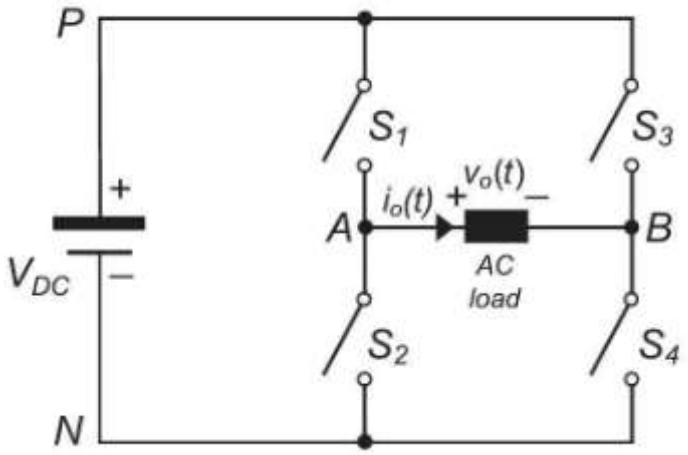


Fig.2 H-Bridge Inverter

The source's higher potential terminal is denoted by the letter "P," and its lower potential terminal by the letter "N." Since the load can be entirely resistive, capacitive, or inductive in nature, it is depicted as a black box. The load requires alternating current for its conduction. When the potential at A is higher than at B, then V_o is regarded as positive, otherwise it is negative. Similarly, when the direction of current is from A to B, then $i_o(t)$ is considered positive, otherwise it is negative. The circuit also has four switching devices S1, S2, S3 and S4. By turning ‘ON’ or ‘OFF’ particular switches we can obtain our desired output voltages.

2.2 Multi-Level Inverters

A multi-level inverter's output waveform has more than two levels. The bulk of industrial applications have started to demand more powerful equipment in recent years. For a number of medium voltage utility and motor driving applications, megawatt power levels and medium voltage are required.

A medium voltage grid cannot be directly linked to a power semiconductor switch. As a result, a multiple power converter structure has been created for use in high power and medium voltage scenarios.

In addition to achieving high power ratings, a multilevel converter also makes it possible to employ renewable energy sources for high-power applications, including photovoltaic cells, wind turbines, and fuel cells.

2.3 Advantages of Multi-Level Inverters

1. Total harmonic distortion (THD) reduces
2. High Voltage level obtained
3. Staircase waveform quality
4. Operates at both fundamental and high switching frequency PWM
5. Low switching losses
6. High power quality
7. Electromagnetic interference reduces
8. They generate less CM, or common-mode voltage. Furthermore, CM voltages can be eliminated using complex modulation techniques.

2.4 Multilevel Inverter Topologies

2.4.1 Diode Clamped Inverter

Diode-clamped topology, also referred to as NPC (Neutral Point Clamped Invert-er) topology, first drew attention when Nabae et al. demonstrated the use of an NPC inverter alongside experimentation utilizing a pulse-width modulation technique in the 1980s [3].

The clamping diode is used for the Diode-Clamped Multilevel Inverter to transmit a minimal quantity of voltage [4]. n2 is the total number of components needed for n-level voltage production, which includes 2*(n-1) IGBT devices linked in series, (n-1)*(n-2) clamping diodes, (n-1) dc link capacitors to split the dc link into various voltage levels, and one dc voltage source [14]. Diode clamped multilevel inverters have a significant disadvantage in that their maxi-mum output voltage is only half of the input dc voltage, but they also have high efficiency due to the fundamental frequency that is used in all switching devices.

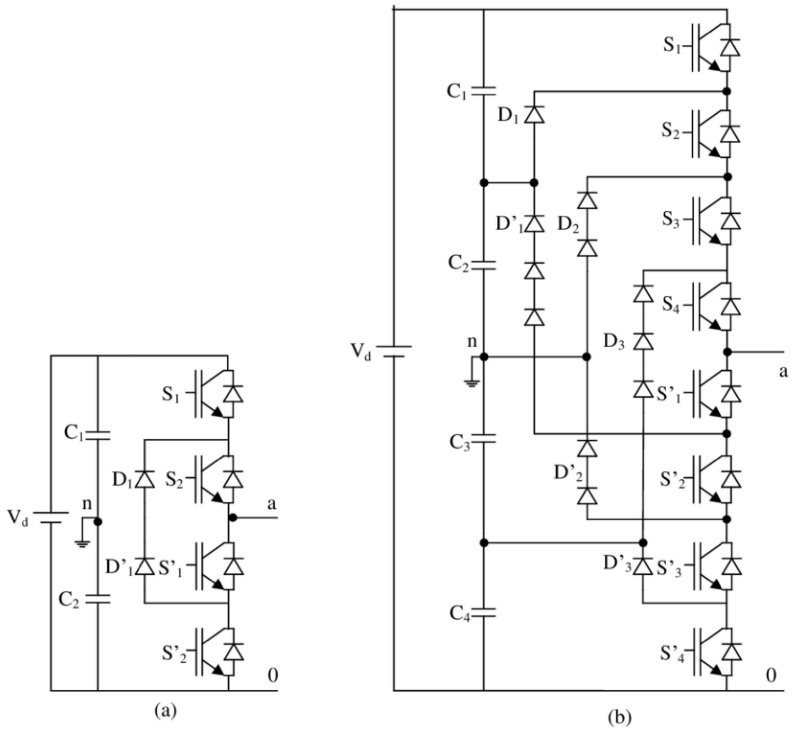


Fig.3 Diode-Clamped MLI

2.4.2 Flying-Capacitor MLI

This inverter's configuration structure is similar to that of the preceding one, with the exception that here, capacitors are employed to limit voltage rather than diodes [5].In order to limit voltage, n level flying capacitor inverters combine (n-1) *(n-2)/2 clamping capacitors and (n-1) DC link capacitors with (2n-2) switching components.

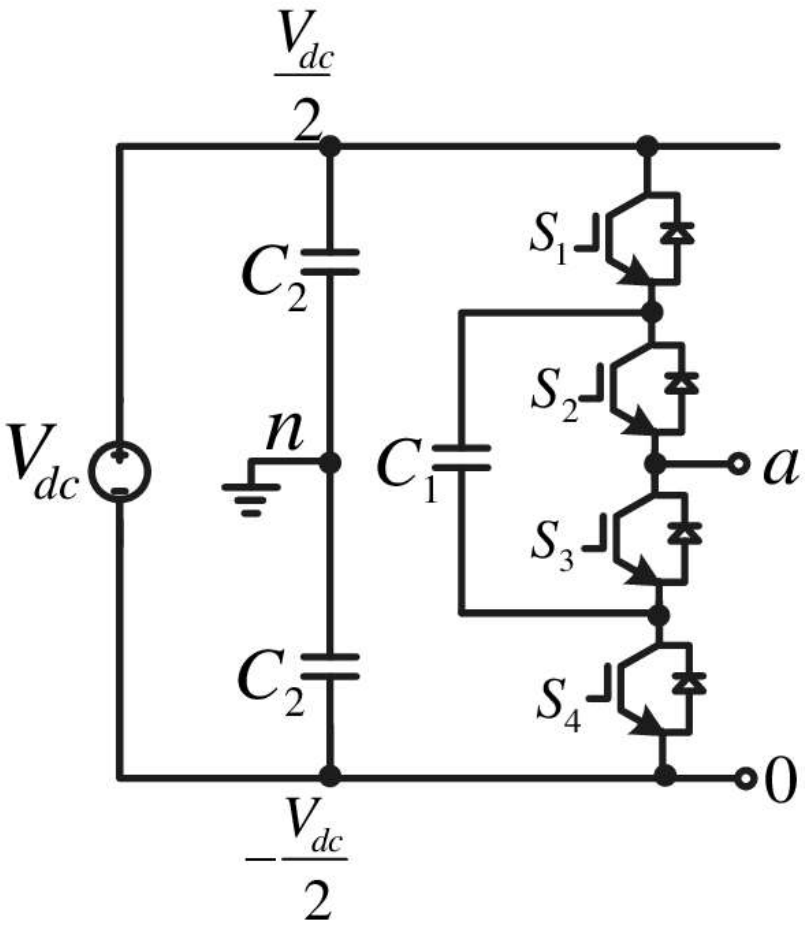


Fig.4 Flying-Capacitor Three-Level MLI

2.4.3 Cascaded H-bridge Multi-level Inverter

The cascaded H-bridged multi-level inverter (CHBMLI) is one of the popular forms of multi-level inverters utilized in high power moderate-voltage circuits.

The construction of the cascade H-bridge is the least complicated of the three multilevel inverter topologies since it uses fewer parts. There are several topologies for cascaded H-bridge multi-level inverters with regard to the input DC voltage source. The first kind of CHB-MLI has equal DC voltage supplies; this form of inverter generates high ac voltages by combining several equal units of the power supply.

A sine wave replica staircase waveform is created using a multilevel inverter. The use of multicarrier PWM techniques further enhances it.

A number of n H-bridge inverter cells make up the cascade H-bridge multilevel inverter. Four primary switches and one distinct dc voltage source are employed in each cell.

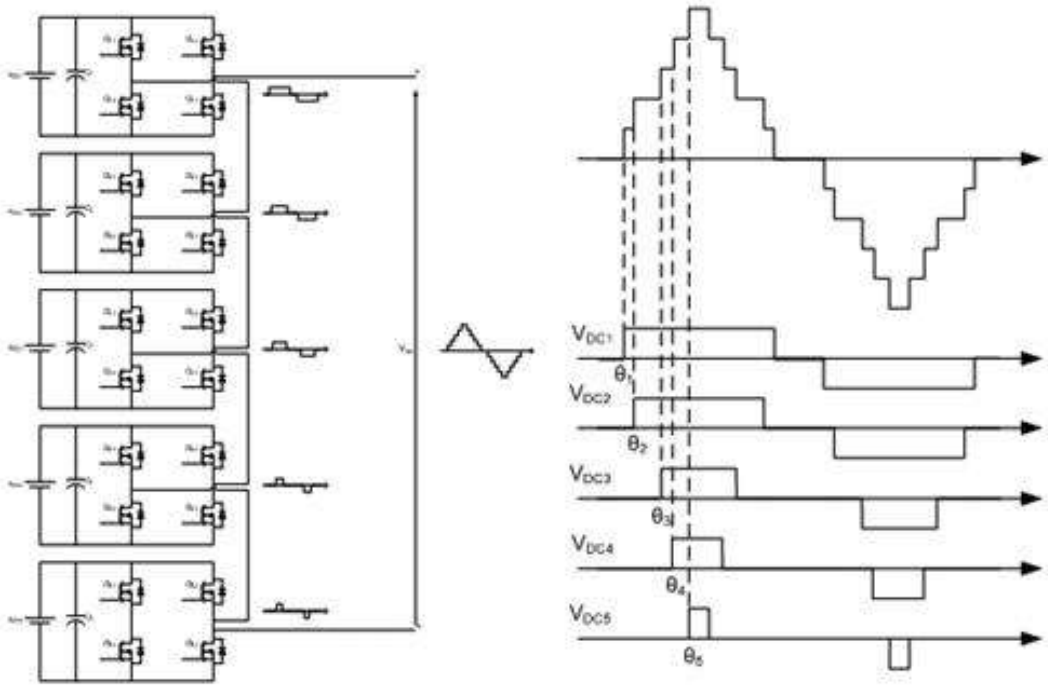


Fig.5 Cascaded H-bridge MLI

2.4 Proposed Topology

Fig. shows the novel multilevel inverter topology for a 15-level Asymmetrical Multilevel inverter that can reduces the count of switching devices. This is a full-bridge DC-AC converter which is having DC voltage source of different magnitude. In Fig.1, For this 15-Level inverter Four DC voltage in which three are of same magnitude and one of different voltage value are required along with 10 IGBTs switches. This topology arrangement of different magnitude voltage sources along with a full-bridge converter gives the 15-level output voltage.

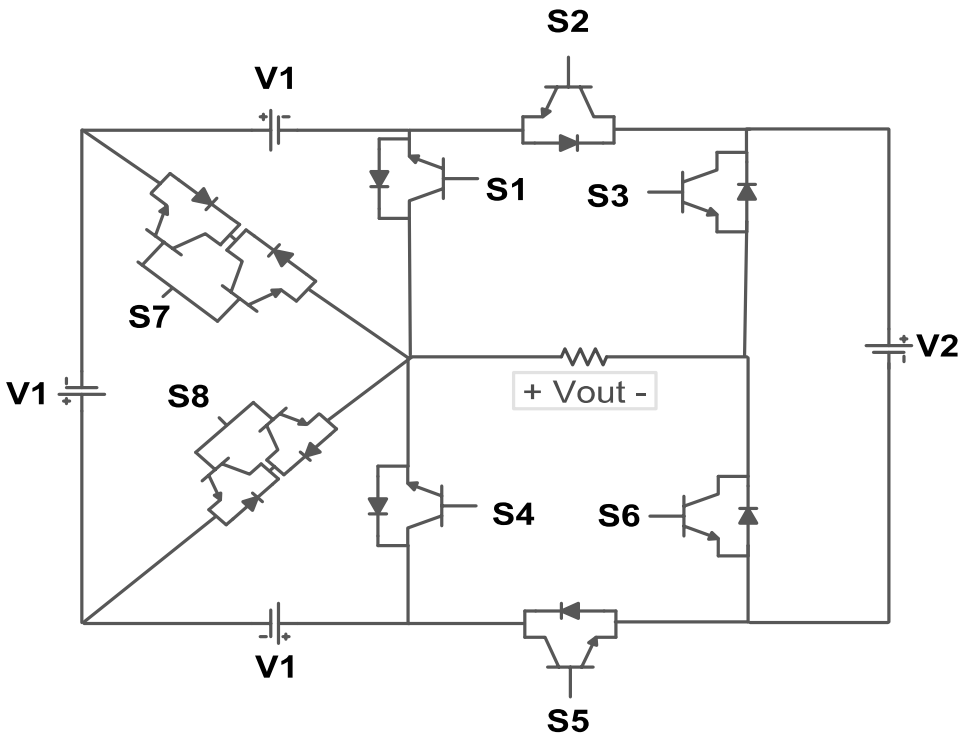


Fig.6 Fifteen Level MLI

The basic multilevel unit of the proposed topology is shown in Fig.1 it is a 15-level inverter. It has four power sources and eight switches. Six of the eight switches have a single orientation, and two are bidirectional. Using an IGBTs and an anti-parallel diode a switch is made. It can prevent one-way current. Using two unidirectional switches we can construct an Bidirectional switch that allow cur-rent to flow in both directions.

Table 1 Switching States under Positive and Negative half cycles

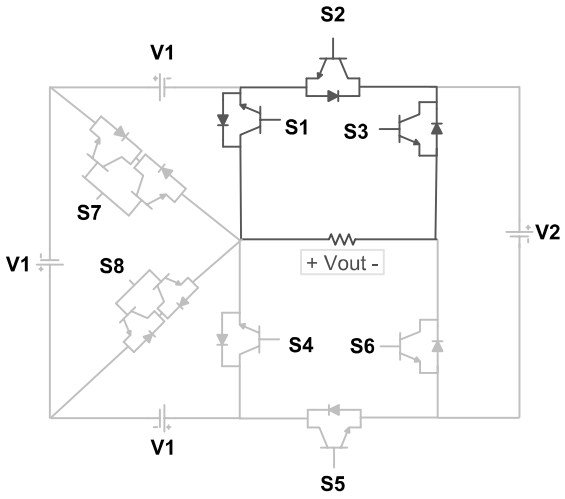
For Positive Cycle:

State	S1	S2	S3	S4	S5	S6	S7	S8	Voutput
0	✓	✓	✓						0
1		✓	✓				✓		V1
2		✓	✓					✓	2V1
3		✓	✓	✓					3V1
4	✓	✓				✓			V2
5		✓				✓	✓		V1+V2
6		✓				✓		✓	2V1+V2
7		✓		✓		✓			3V1+V2

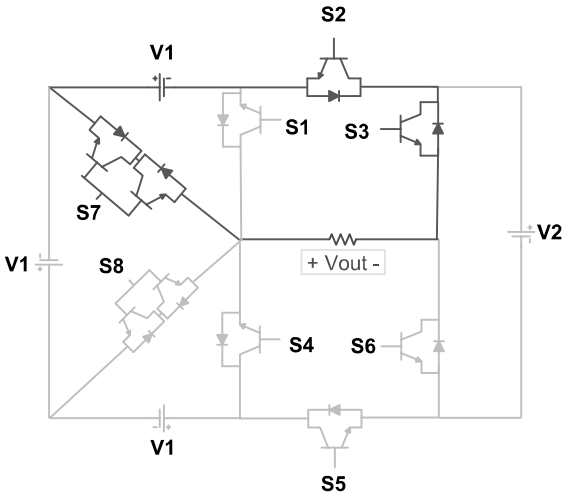
For Negative Cycle:

State	S1	S2	S3	S4	S5	S6	S7	S8	Voutput
0				✓	✓	✓			0
1					✓	✓		✓	-V1
2					✓	✓	✓		-2V1
3	✓				✓	✓			-3V1
4			✓	✓	✓				-V2
5			✓		✓			✓	-(V1+V2)
6			✓		✓		✓		-(2V1+V2)
7	✓		✓		✓				-(3V1+V2)

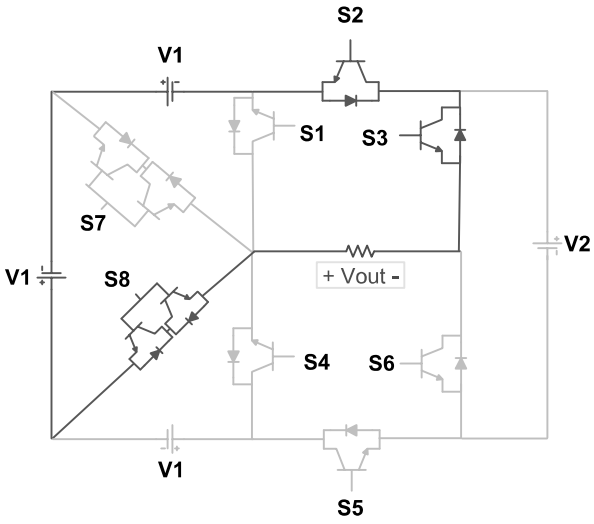
From Table 1.1, switches S3 and S6 operate in a manner opposite to each other, meaning that if one switch is on for a certain voltage level, the other must be off. To prevent the dc supply from shorting, this is essential. Switches S2 and S5 operate in a pair that complements likewise. Fig. 2 demonstrates the different levels obtained using different switching modes.



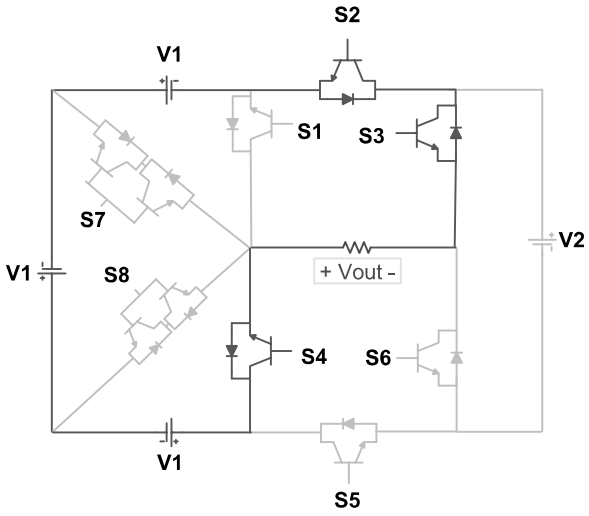
Stage: 0



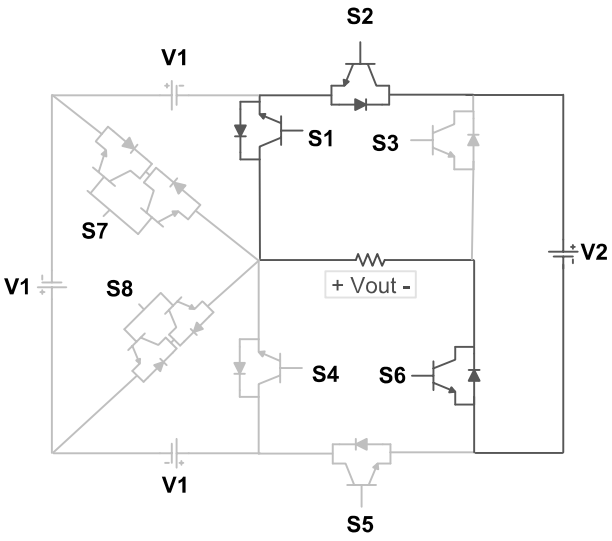
Stage: 1



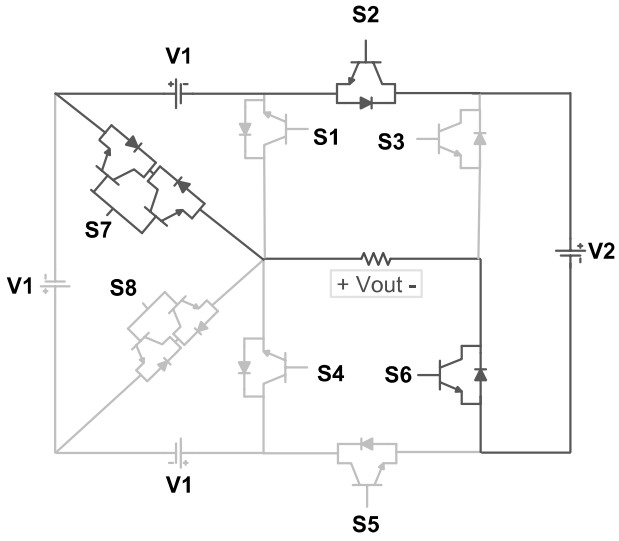
Stage: 2



Stage: 3



Stage: 4



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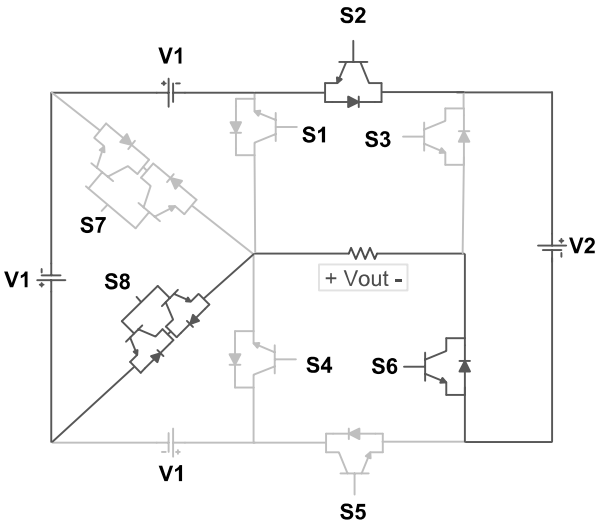
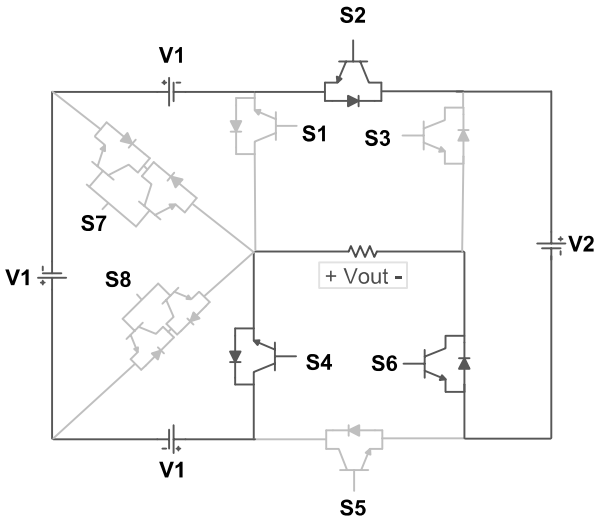


Stage: 6



Stage: 7

Fig.7 Different switching modes

2.5 Voltage Rating Of Switches

The rating of the switches has an indirect impact on the inverter's price. The highest voltage that the switch can block determines the switch's rating. TSV is the collective name for all of the switches' blocking voltages. The maximum blocking voltages for various switches in the proposed basic multi-level unit are listed below:

$$E_{S3}=E_{s6}=V_2; \quad (1)$$

$$E_{s2}=E_{s5}=(V_2+3V_1); \quad (2)$$

$$E_{s1}=E_{s4}=3V_1; \quad (3)$$

$$E_{s7}=E_{s8}=4V_1; \quad (4)$$

$$TSV=2\times(V_2+(V_2+3V_1)+3V_1+4V_1)=4(V_2+5V_1) \quad (5)$$

It is obvious from the expression above that the TSV value is dependent upon the parameters of the DC voltage sources and is simple to compute. For instance, dc source values in the 15-Level structure are in the ratio V2:V1 = 4:1. Consequently, in this instance, the TSV will be

$$TSV=2\times(V_2+(V_2+3V_1)+3V_1+4V_1)=4(V_2+5V_1)=36V_1 \quad (6)$$

The term $TSV_{p.u.}$ refers to the ratio of TSV to maximum output voltage. (TSVp.u .) will be

$$TSV_{p.u.}=\frac{36}{7}=5.14 \quad (7)$$

CHAPTER-III

3.1 Universal Control Scheme

The proposed control strategy is described in this section. It is designed in such a way that it may be used with any multilevel inverter topologies. Let N level be the total number of levels in the phase voltage for the provided inverter. If N level>3, a voltage source inverter can operate at several levels. Level 0 is significant; hence N level is regarded as unusual. The N level waveform's number of positive levels will also be:

$$N = (N_{level} - 1)/2$$

A sinusoidal waveform of amplitude Aref and frequency $\boldsymbol{f_{ref}}$ constitutes the modulating signal $\boldsymbol{a_{ref}(t)}$ [4]. For sine PWM and low-frequency schemes, there needs to be triangular, constant, 2N carrier signals. The frequency of these carriers is$\boldsymbol{fcar}$, and Acar is their peak-to-peak amplitude. Carrier signals that are higher than the zero level are known as $\boldsymbol{a^{+}_{car,j}(t)}$ and those that fall below the zero level are known as$\boldsymbol{a^{-}_{car,j}(t)}$, $\boldsymbol{(j = 1 \text{ to } N)}$. The zero reference is positioned in the middle of the continuous bands that the carrier signals occupy.

Accordingly, the following quantities can be defined:

Index of frequency modulation, $\boldsymbol{P = Acar/(Aref)}$

"P" determines the output waveform's harmonic profile as well as the power switches' switching frequency.

Index of amplitude modulation, $\boldsymbol{M = Aref/(NAcar)}$

The output waveform's peak value and the number of levels are determined by the value of "M". Each carrier is compared against the modulating signal at every instant. For each comparison, the result is either "1" if the signal that is being modulated is more than the carrier, or "0" if it is not. This applies to all carrier signals above the zero reference. For each comparison, the result is either "0" if the modulating signal is greater than the carrier or "-1" if the carrier signal is less than the zero reference. That is.

$$a^{+}_{out,j}(t) = 1, \qquad for\ a_{ref} \geq a^{+}_{car,j}(t)$$

$$=0, \qquad \text{otherwise}$$

$$a^{-}_{out,j}(t) = 0, \qquad for\ a_{ref} \geq a^{-}_{car,j}(t)$$

$$= -1, for\ otherwise$$

The results so obtained are combined to create an "Aggregated signal" that is designated as $\boldsymbol{a_{agg}(t)}$.

That is,

$$a_{agg}(t) = \sum_{j=1}^{N} (a^{+}_{out,j}(t) + a^{-}_{out,j}(t))$$

It should be observed that the wave shape of $a_{agg}(t)$ gains the same property as the anticipated output voltage. With a certain topology, power electronic switches require real-world driving signals, which requires the use of logical components and a look-up table to be generated from $a_{agg}(t)$. Using Boolean operations,

$$a_{d,t}(t)\ are\ derived\ from\ a_{agg}(t)\ using\ following\ criteria:$$

$$a_{d,t}(t) = 1, if\ a_{agg}(t) = j$$

=

$0, otherwise;\ where, j = -N\ to\ +N$

As a result, a total of N-level derived signals will be produced, each of which will be used to operate the switches that must remain ON at the voltage level indicated by the output waveform. In order to acquire the switching function $a_{switching}(t)$ for a certain switch, the necessary derived signals would be sent into an OR gate. The block diagram is shown in fig.3 .The mathematical formulation of the switching function is

$$a_{switching}(t) = \overline{\prod \overline{a_d(t)}}$$

Where,

$$\overline{a_d(t)} = 1 - a_d(t)$$

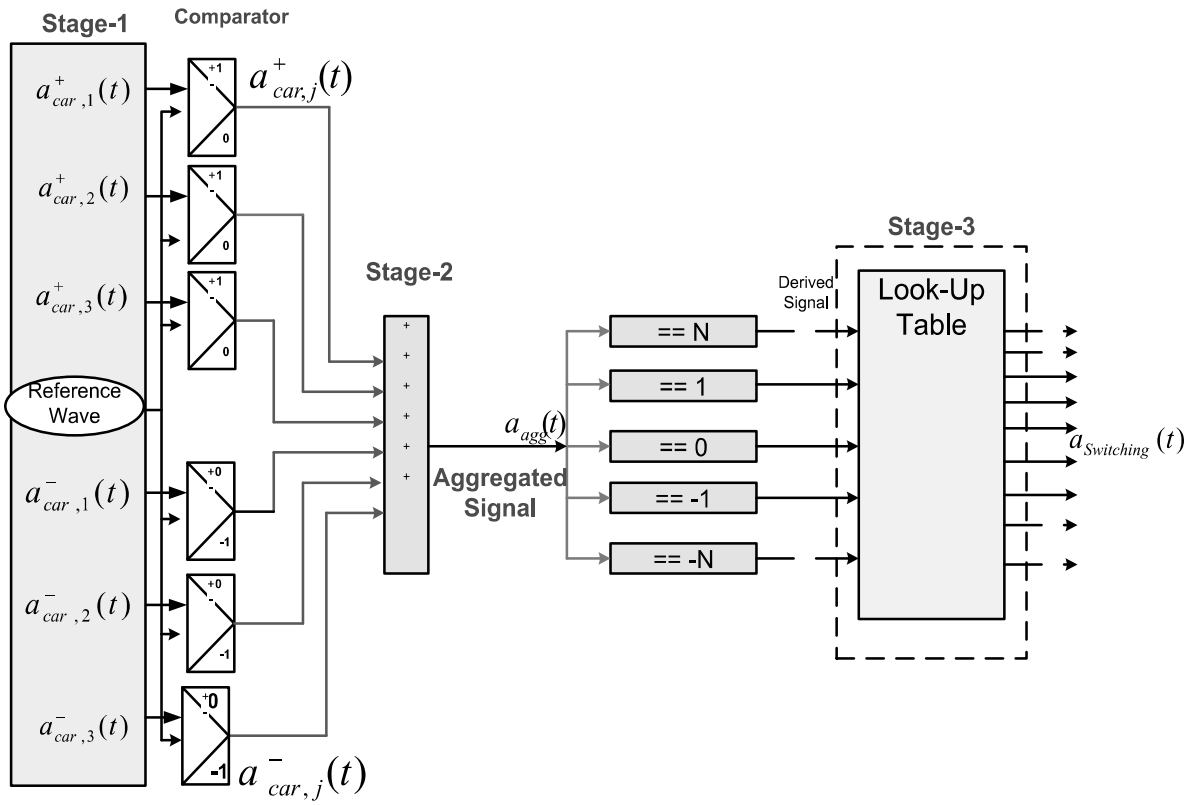


Fig.8 Block Diagram Of Universal Control Scheme

3.2 Control and Modulation Techniques in Proposed Topology:

For MLIs, some modulation techniques have been presented down in the literature. PWM techniques use many levels of carriers offset between the carriers. Moreover, the reference wave (modulating signal) allows for the injection of zero sequence signals as well as freedom in frequency, amplitude, and phase angle. As a result, numerous multilevel carriers-based PWM techniques can be obtained by using these combinations. Typically, n -1 carrier signals are needed for an inverter with n levels in the phase voltage. Multi-carrier PWM techniques are as follows:

3.2.1 Phase Disposition PWM

The full (N-1) carrier is in phase and has the same amplitude and frequency in PD PWM. Fourteen carrier waves are used in this proposed topology in comparison to a single sine reference wave. When employing MLI, N-voltage levels are represented by N-1 carrier signals. The PD PWM method is depicted in Fig.

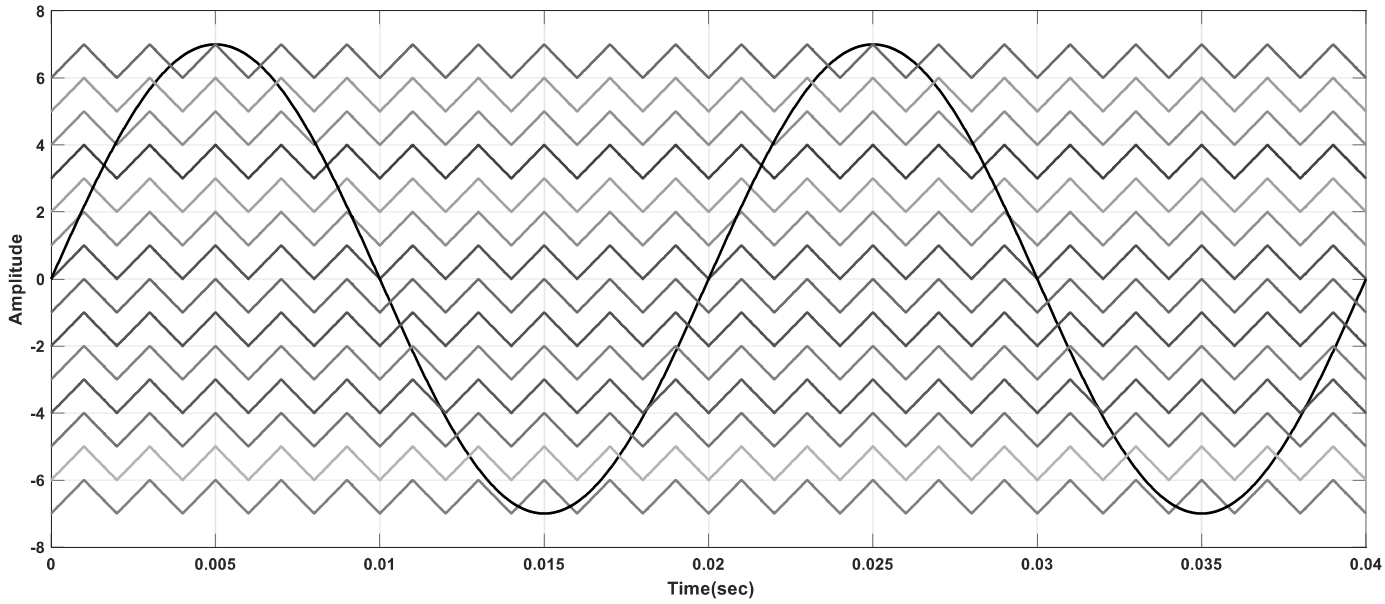


Fig.9. PDPWM

3.2.2 Phase Opposition Disposition PWM (PDPWM)

The carrier signal in this system are phase-locked to each other both below and above the zero reference, but as shown in Fig.10 , the carrier signals below and above the zero reference are phase opposition with each other.

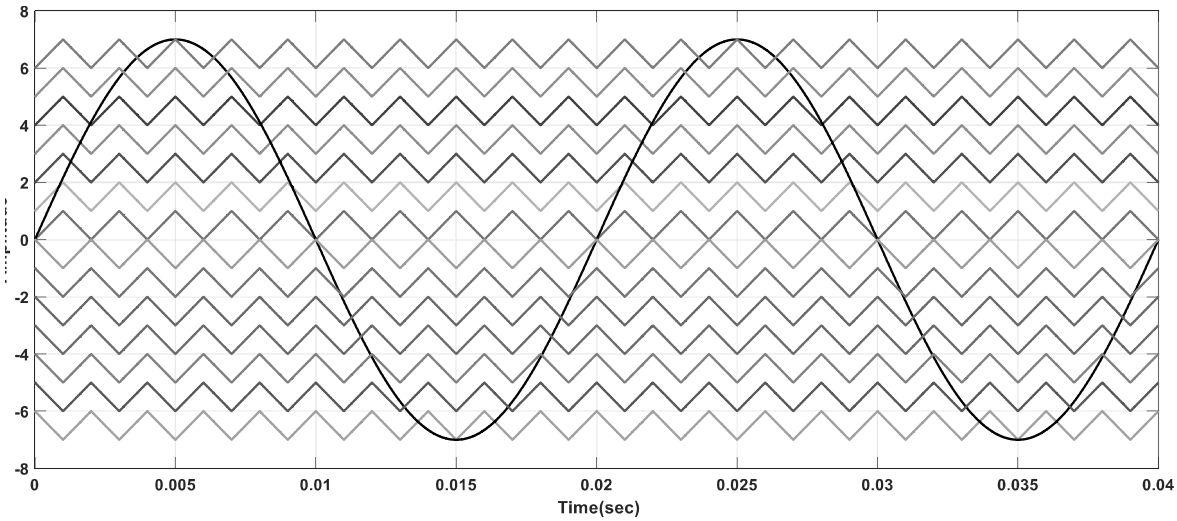


Fig.10. PODPWM

3.3.3 Alternate Phase Opposition Disposition (APODPWM) PWM

In this technique, the carrier signals are alternately phase-displaced by 180 degrees from each other, as shown in Fig.11.

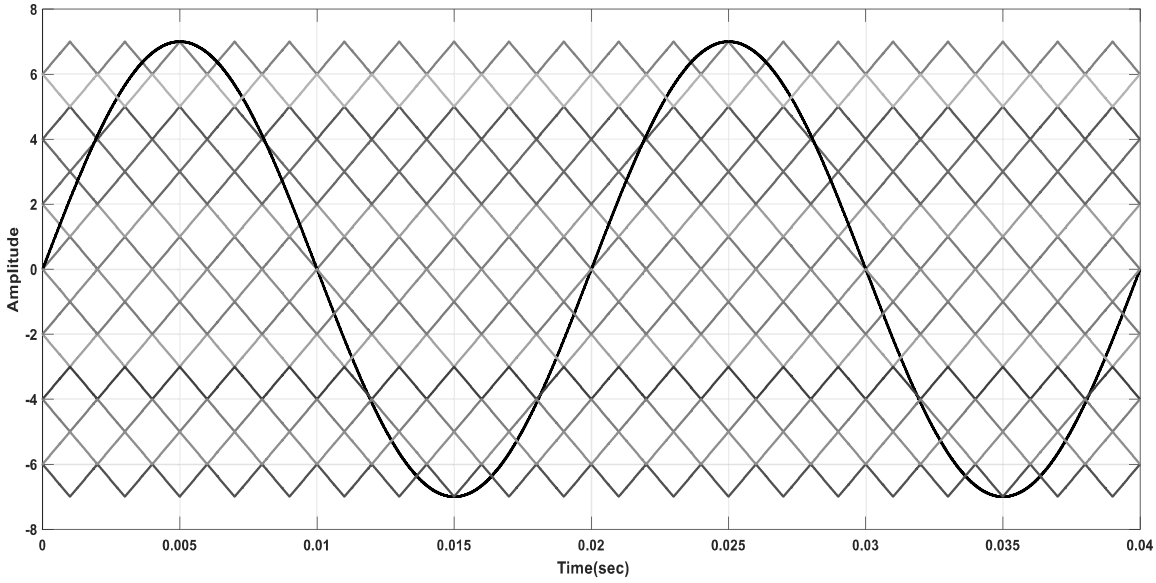


Fig.11.APODPWM

3.3.4 Variable Frequency PWM(VFPWM)

All of the carrier waves in variable frequency pulse width modulation have different frequencies with respect to one another, as demonstrated in Fig.12.

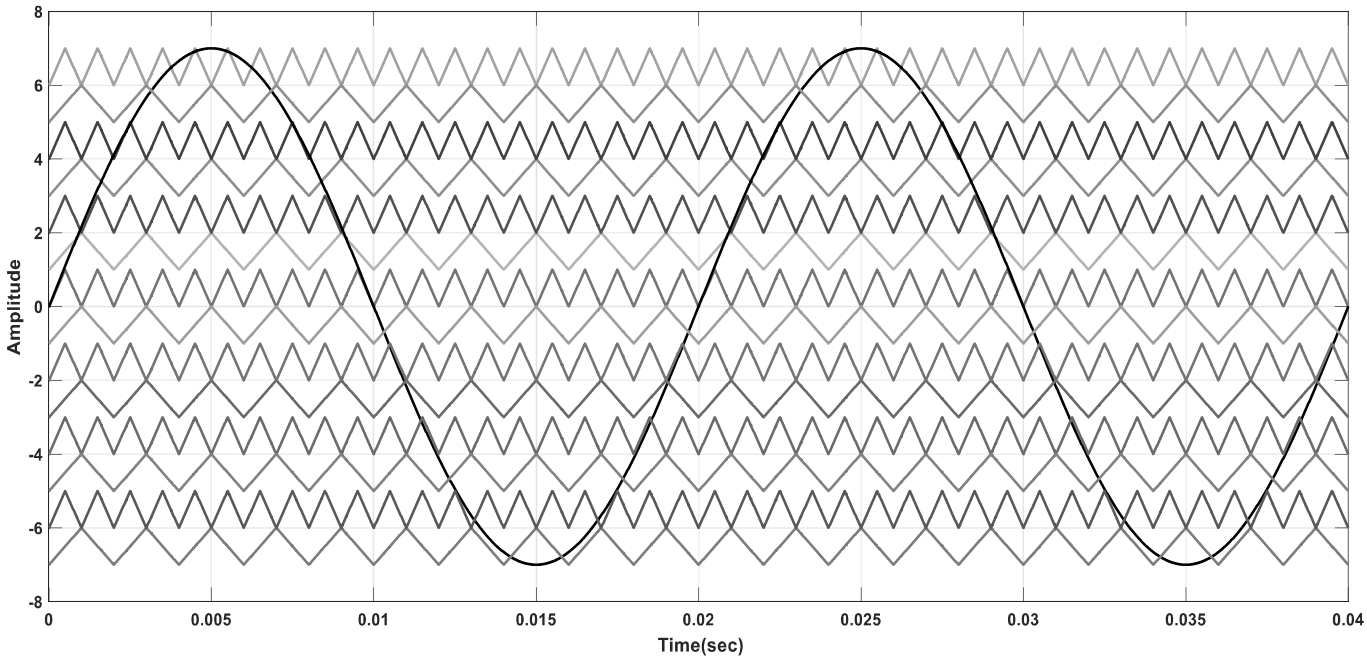


Fig.12 VFPWM

3.3.5 Inverted Sinusoidal Carrier PWM

In this technique, a sine wave is used as a carrier wave. The inverted sine carrier PWM (ISCPWM) technique uses an inverted sine carrier with a high frequency as the carrier signal and a sine wave as the reference signal. Low harmonic distortion is produced by the combination of reference and carrier signals with varying modulation indexes [16].

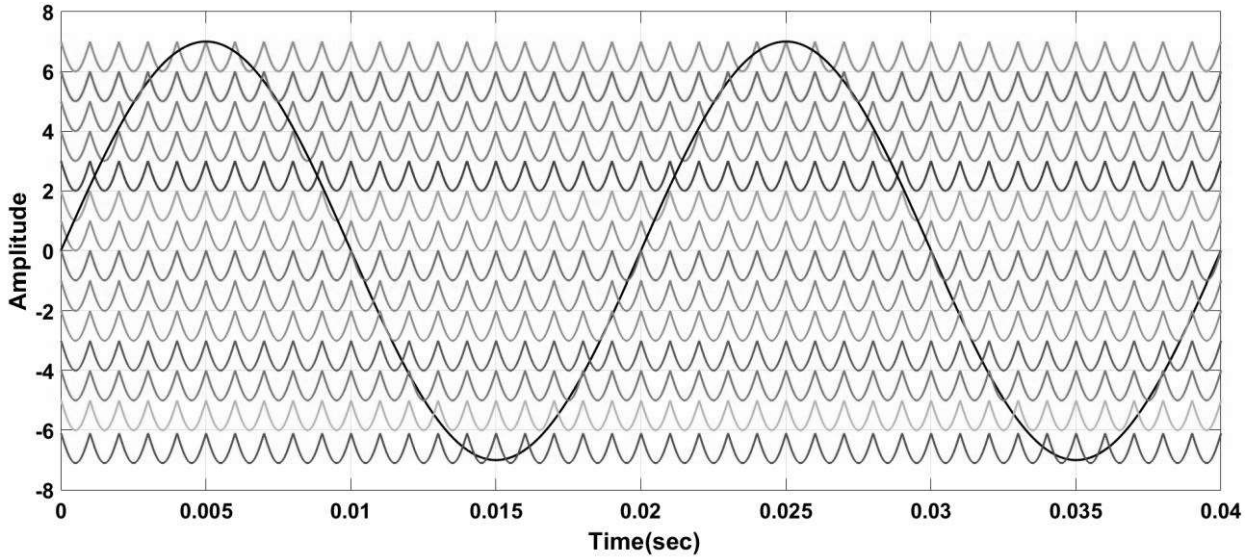


Fig.13. ISCPWM

3.4 Variable Frequency Inverse Sinusoidal Carrier PWM (VFISCPWM)

In this technique, two inverted sinusoidal carrier signals having frequency different from each other are taken to compare with the sinusoidal reference wave as demonstrated in Fig.14 [14].

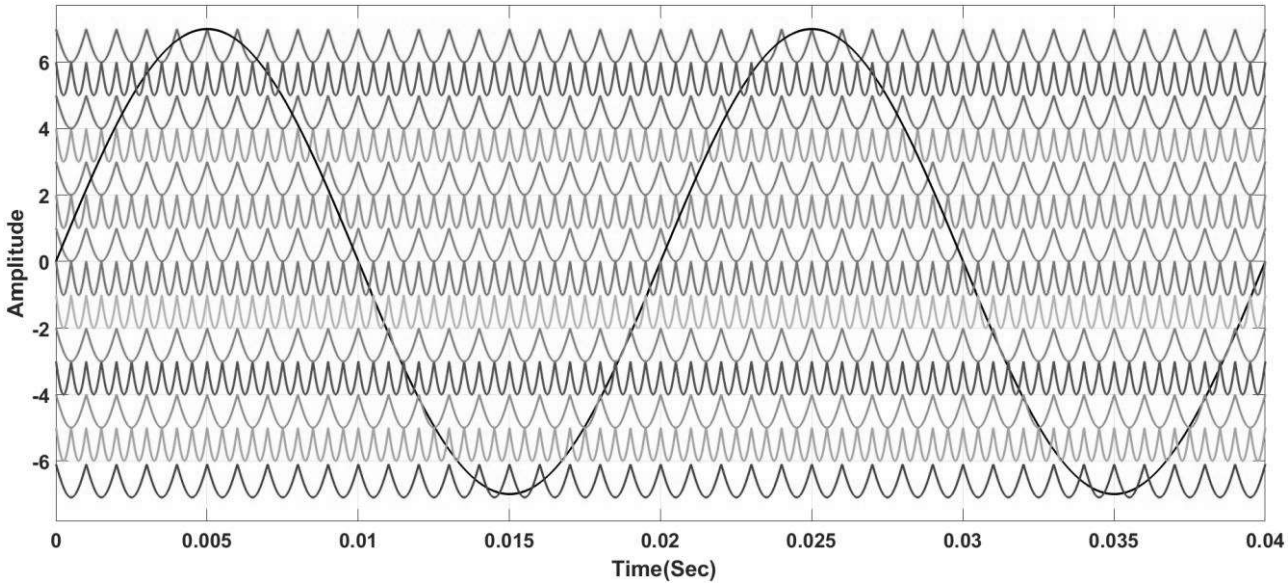


Fig.14. VFISCPWM

3.3Simulation

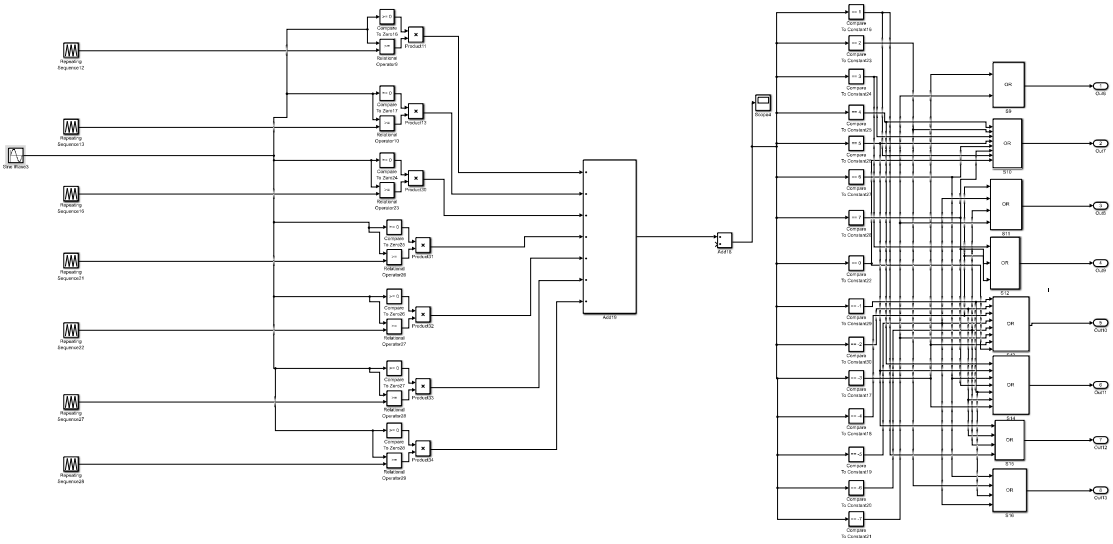


Fig.15 Universal Control Technique Triggering Circuit (Simulink)

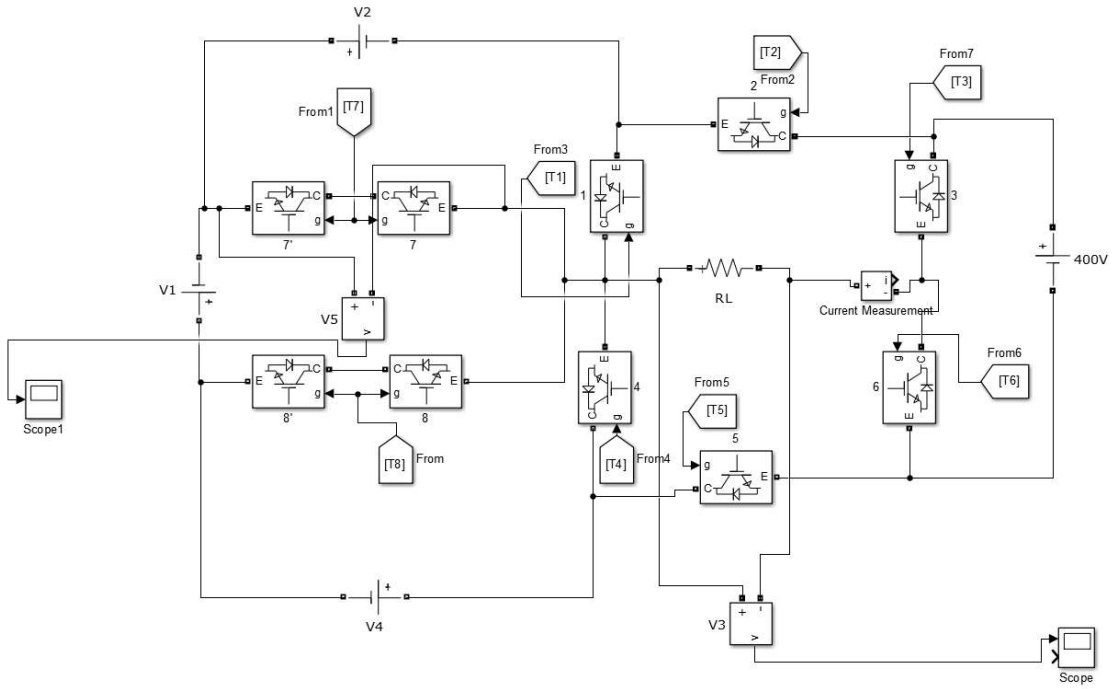


Fig. Proposed Topology in Simulink

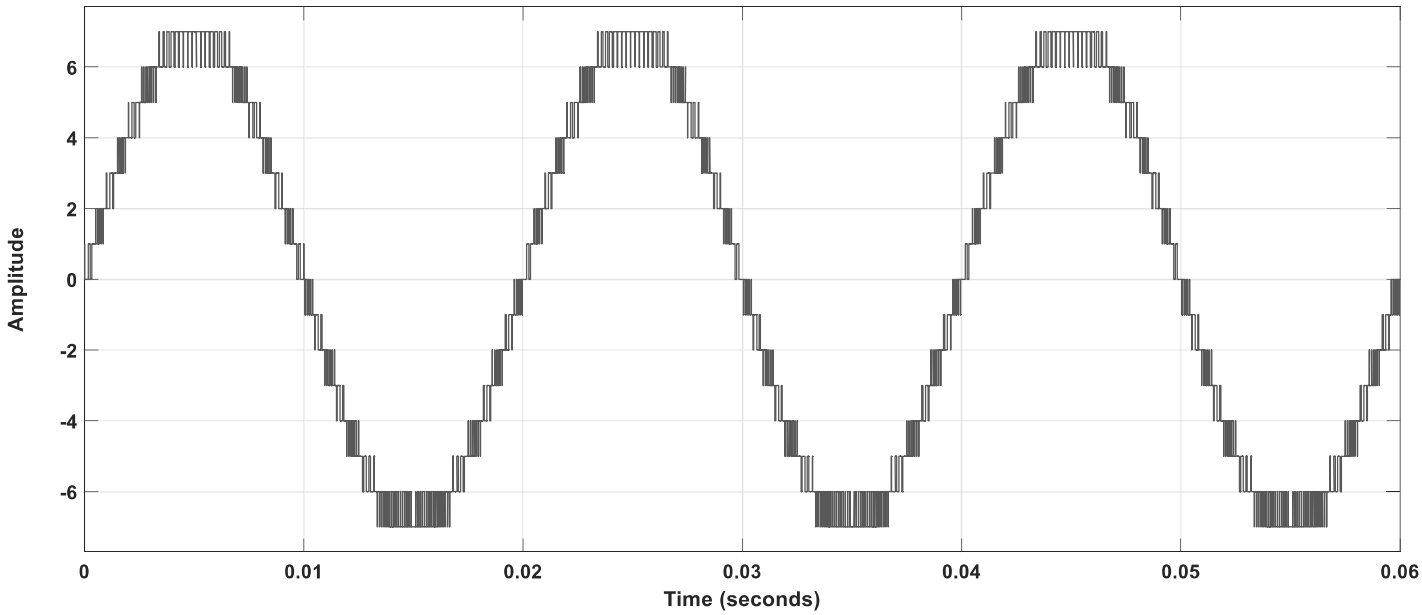


Fig.16 Fifteen Level Triggering

CHAPTER-IV

RESULTS AND DISCUSSION

4.1 Simulation Results

Using MATLAB/SIMULINK R2016a software, the performance of the suggested topology was evaluated. The simulation has assumed the switches to be lossless. A high switching frequency approach with a carrier frequency of 10 kHz is employed in this study [15]. This paper uses six PWM approaches, including PD, POD, APOD, VFPD, ISC and VFISC, with various modulating indices. The simulation parameters are as follows: R= 40-ohm, DC voltage source V1= 100V and V2 =400V; carrier signal frequency is 10 kHz.

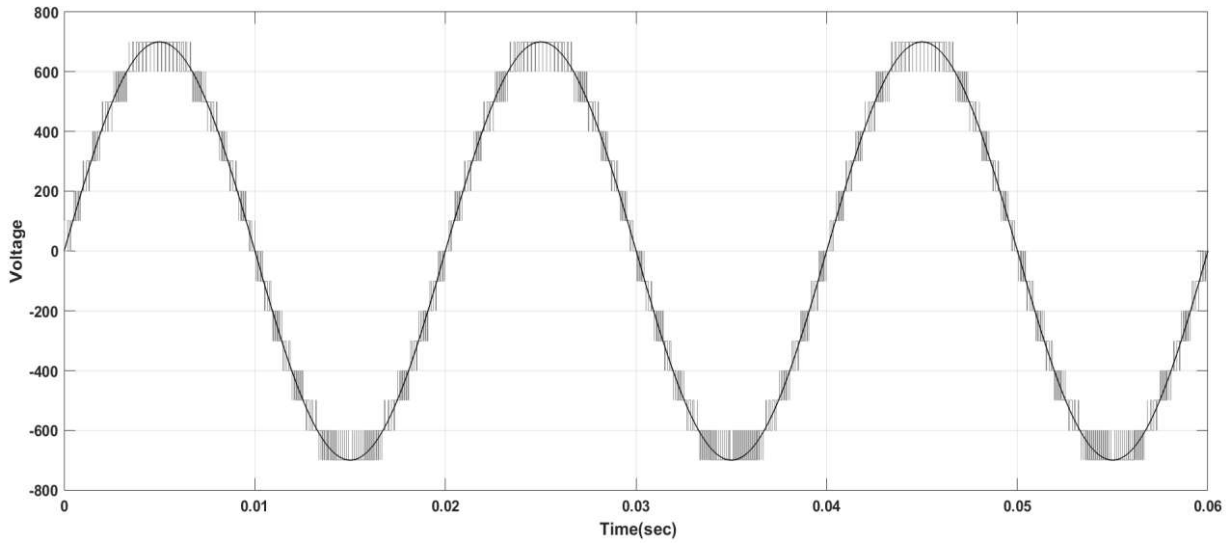


Fig.17 Output Voltage Waveform of Fifteen-Level Inverter

4.2 FFT Analysis

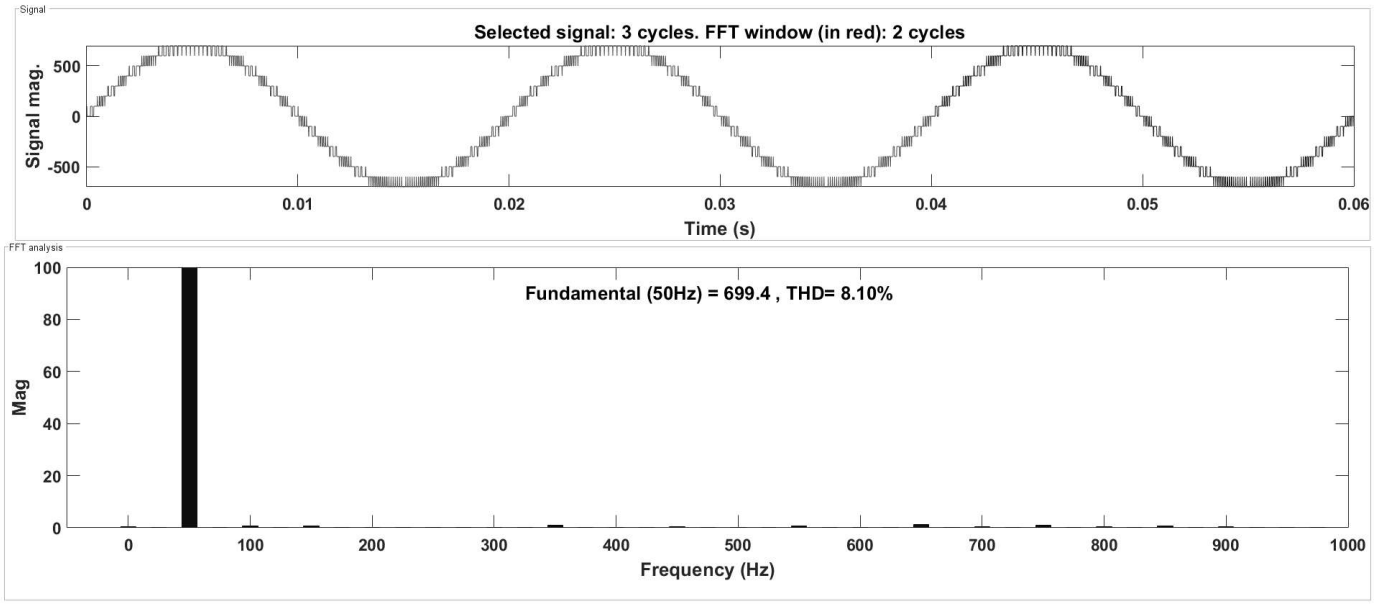


Fig.18 FFT Analysis of Voltage Signal

4.3 FFT Analysis of Different Techniques

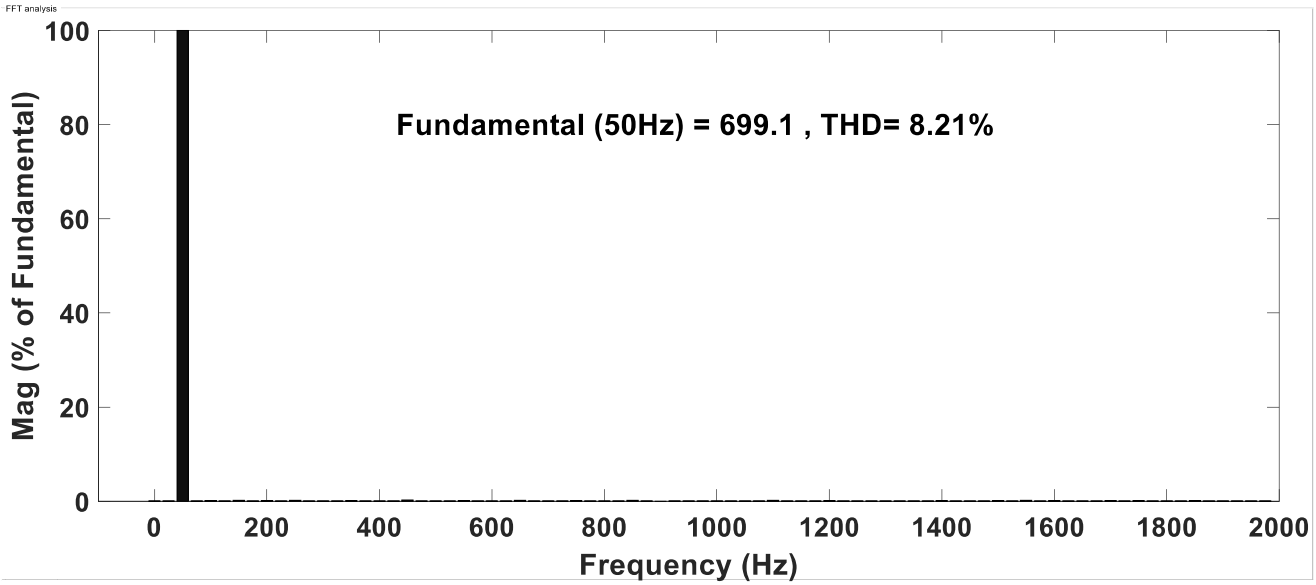


Fig.19. THD in PDPWM Technique

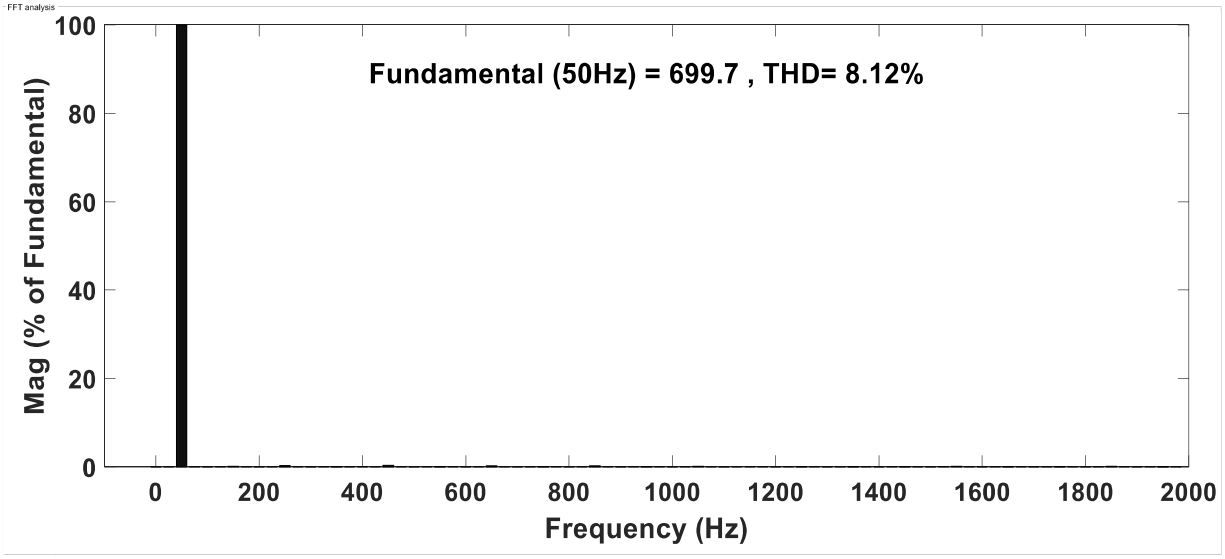


Fig.20. THD in PODPWM Technique

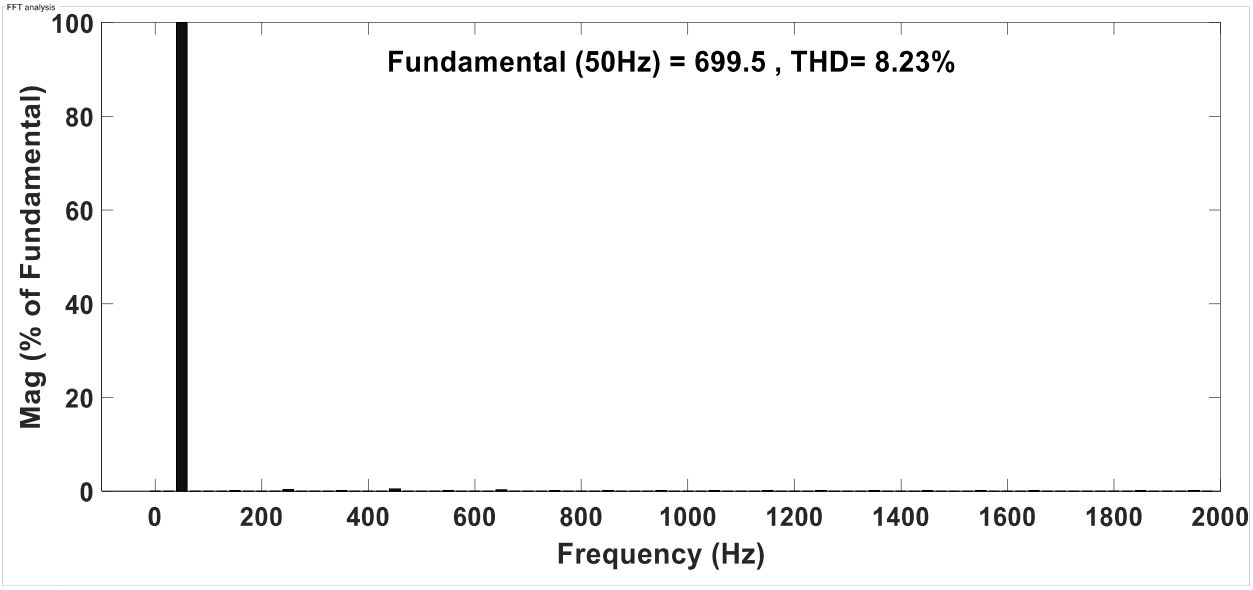


Fig.21. THD in APODPWM Technique

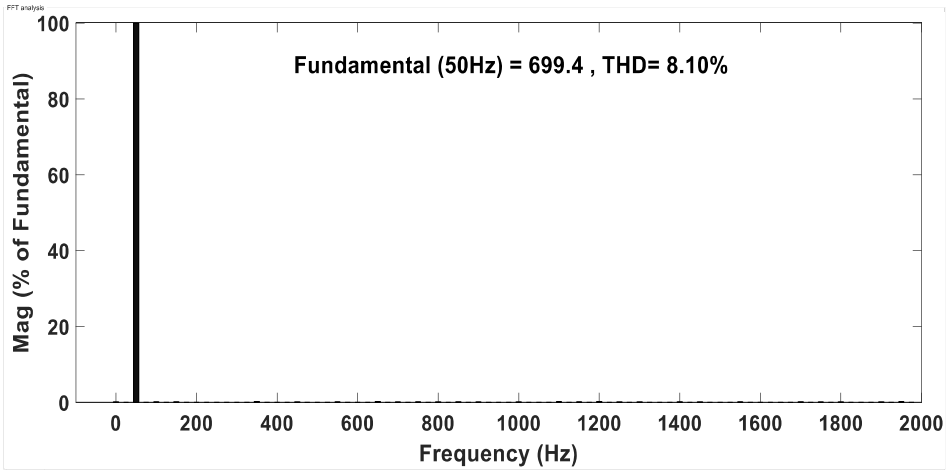


Fig.22. THD in VFPDPWM Technique

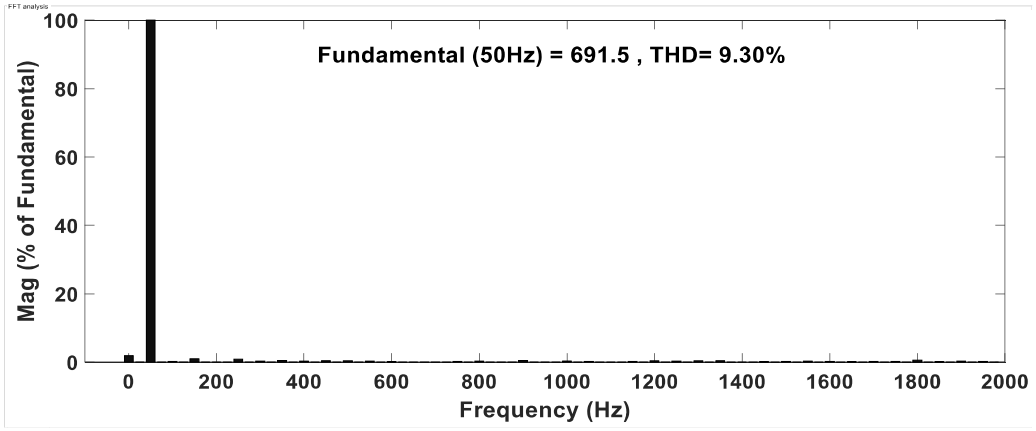


Fig.23. THD in ISCPWM Technique

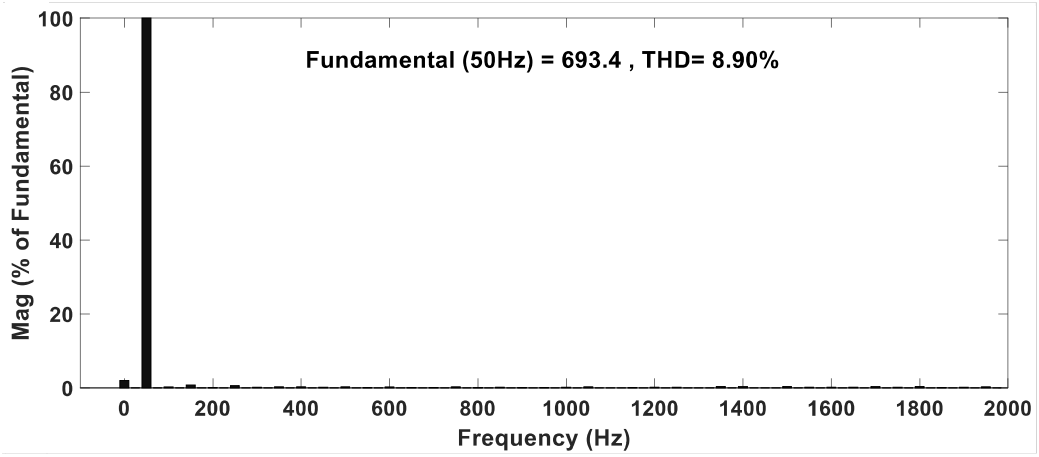


Fig.24. THD in VFISCPWM Technique

Table 2 THD Comparison of the Proposed MLI Topology using Various PWM Techniques under varying modulation index

Level	Modulation Index (Ma)	Modulation Technique					
		PD	POD	APOD	VF	ISC	VFISC
15	1.1	7.86	7.85	7.95	7.70	8.74	8.63
	1	8.21	8.12	8.23	8.10	9.30	8.9
	0.9	8.46	8.49	8.45	8.46	9.31	9.10
	0.8	8.9	8.94	8.85	8.81	9.37	9.20

Table 3 Comparison of multiple MLI topology

Inverter Topologies	CHB	NPC	Flying-Capacitor	Proposed Topology
IGBTs/Switching Devices	28	28	28	8
Diodes	0	0	0	0
Clamping Diode	0	182	0	0
DC bus capacitor	0	14	14	0
Flying capacitor	0	0	91	0
DC source	7	1	1	4

4.4 Experimental Results & Discussion

In the paper, the universal control techniques have been implemented to control the MLI. Six different PWM modulations techniques have been presented on varying modulation index. In experimentation, a low cost STM32F4 discovery board haven been used to verify universal technique experimentally. The experimental photograph is shown in Fig. 14. The discovery board has ARM Cortex-M4 32-bit microcontrollers installed and have fifteen analog to digital pin (PA0-PA7, PB0-PB1 and PC0 to PC5), two digital to analog pins (PD0-PD1). In this paper DAC pins

are used to extract the outputs of multilevel inverter. Real-time implementation of created Simulink models can be readily created and loaded into the board memory by using Keil, STM32F4 embedded coder target, together with other useful tools.

Create a model using Simulink that includes embedded target blocks in accordance with the applications and accessibility requirements. Before creating any files for Simulink models, ensure that the primary directory path is correctly located in MATLAB's command window. Simulink models can be created and executed on a discovery kit by using the Support packages for STMicroelectronics' STM32F4 exploration board. Integrated into the support package are Simulink blocks for setting and gaining access to board's auxiliary devices. The STM32F4 blocks' third-party interface, in addition to MATLAB, is Waijung soft-ware. The user must install the STM link utility driver before they can finish in-stalling the Waijung block. Choose the parameters for the target arrangement based on your requirements. FIG. 25-27 displays the experimental findings at various modulation indices.

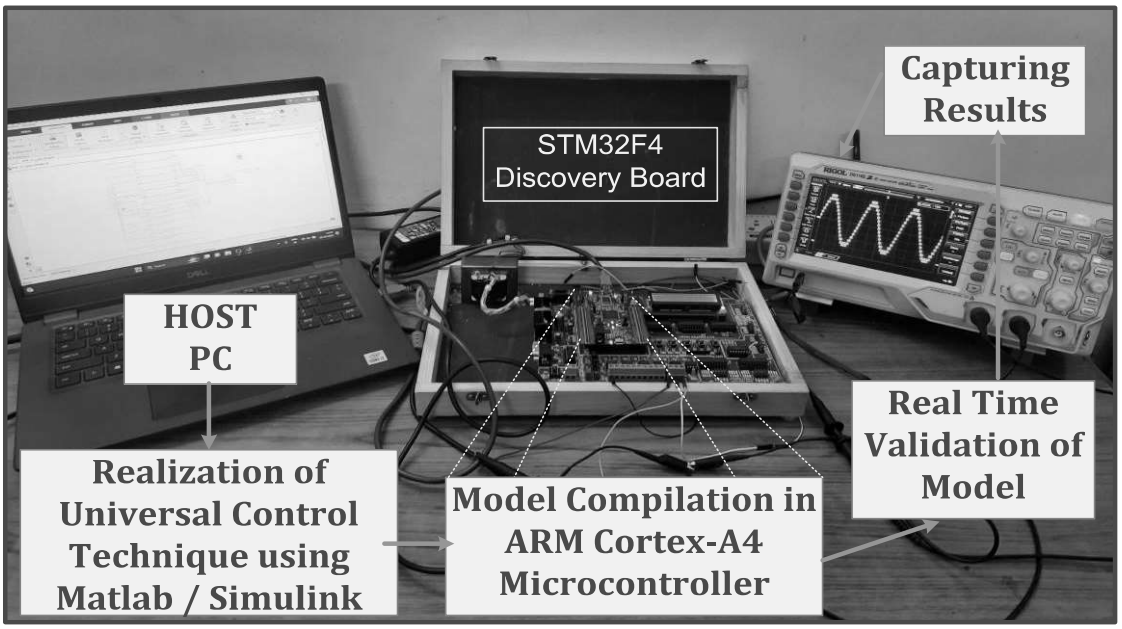


Fig.25 Experimental Realization of Universal Control Technique

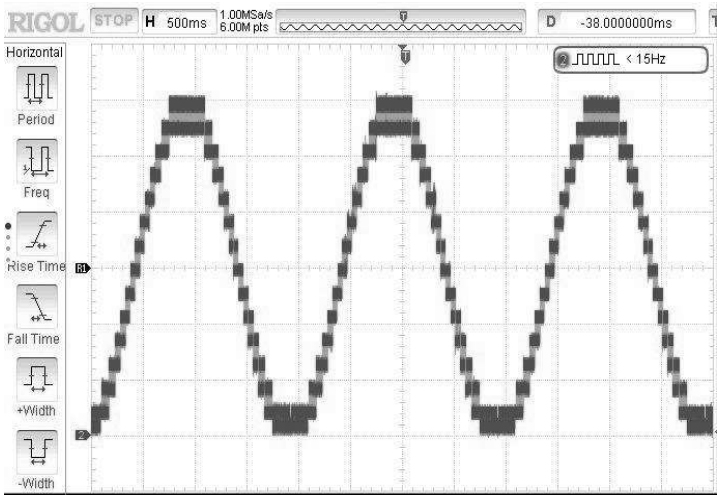


Fig.26 Experimental Output Voltage at modulation index of 1

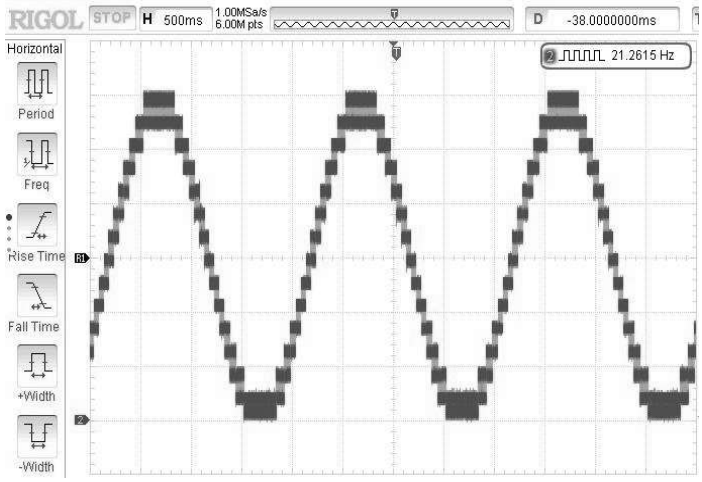


Fig.27 Experimental Output Voltage at modulation index of 0.9

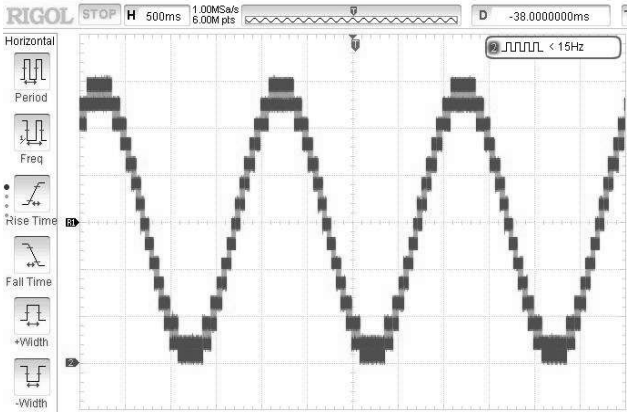


Fig.28 Experimental Output Voltage at modulation index of 0.8

4.5 Conclusion

This work proposes a universal control technique that may be applied to any multilevel inverter topology to achieve a specific modulation strategy. Simulated tests are used to validate proposed concepts. Additionally, it has been demonstrated that the strategy may equally distribute the load among the various DC input sources. According to the comparative evaluation, the suggested 15-level topology has a lower minimum TSV_{pu} than other studied topologies and requires the fewest switches per level. This verifies the superiority and efficacy of the suggested 15-level structure.

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