A PROJECT REPORT

ON

"Series parallel switching multilevel inverter (11 level 15 level and 19 level multilevel inverter)"

SUBMITTED TO -

MADHAV INSTITUTE OF TECHNOLOGY AND SCIENCE GWALIOR

(A Govt. aided Autonomous Institute under RGPV, BHOPAL(M.P.) Established. in 1957)

IN PARTIAL FULFILLMENT FOR THR REQUIREMENT FOR THE AWARD OF THE DEGREE OF

BACHELOR OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

2021

GUIDED BY-

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CERTIFICATE

This is to certify that the major project entitled **"series parallel switching multilevel inverter (11 level 15 level and 19 level multilevel inverter) " which** is being submitted by Love Damor in partial fulfilment for the award of the degree of BACHELOR OF ENGINEERING IN ELECTRICAL ENGINEERING UNDER RGPV, BHOPAL (State Technological University of M.P). It is a record of their own work carried under my guidance and supervision. To the best of my knowledge, the matter present in this major project is original work and has not been submitted anywhere for the award of any other diploma or degree certificate.

Under the Guidance of

PROF. PRAVEEN BANSAL PROF**. NIPUN GUPTA**

Dr. LAXMI SHRIVASTAVA(Head of department)

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ACKNOWLEDGEMENT

I take great pleasure in expressing my deep sense of gratitude to my esteemed institute **MADHAV INSTITUTE OF TECHNOLOGY AND SCIENCE, GWALIOR (M.P)** for providing us the opportunity to fulfill my project.

I gratefully acknowledge with heartfelt gratitude and profound indebtness towards my esteemed project mentor **Prof. Praveen Bansal** and co-guide **Prof. Nipun gupta** for their valuable help and encouragement given throughout the thesis of project.

I gratefully acknowledge with heartfelt gratitude to **Dr. Laxmi Shrivastava** (Head, Department of Electrical Engineering) for her active and productive guidance throughout the whole span of time.

I also acknowledge with gratitude to our director **Dr. R.K. Pandit** for providing the facilities needed for the accomplishment of this project.

The environment at MITS has been valuable experience for us. It has provided an opportunity to learn at our own pace in discipline of interest. The present project is an ample testimonial of the face. Lastly, I would like to thank all those who helped me during different stages of completion of this project as without them it would not have been possible.

MADHAV INSTITUTE OF TECHNOLOGY AND SCIENCE GWALIOR

(A Govt. aided Autonomous Institute under RGPV, BHOPAL(M.P.) Established.in 1957)

2021

DECLARATION

We hereby declare that the work is being presented in the project entitled **"series parallel switching multilevel inverter (11 level 15 level and 19 level multilevel inverter)**" in partial fulfilment of requirement for the award of the degree BACHELOR OF TECHNOLOGY IN ELECTRICAL ENGINEERING at MADHAV INSTITUTE OF TECHNOLOGY AND SCIENCE , GWALIOR (M.P) is an authenticated record of our work carried under supervision of Prof. Praveen Bansal sir, Associate Professor and Prof. Nipun gupta sir, Associate Professor .

We have not submitted the matter embodied in this project for the award of any degree or diploma anywhere else.

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11-level, 15-level and 19-level multi-level inverter

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ABSTRACT

In dissertation work, a 11-level, 15-level and 19-level multi-level inverter is proposed with series parallel switching multilevel inverter (SPSMLI) topology which improves the multilevel performance by compensating the disadvantages (such as increased number of components, complex pulse-width modulation controlling method, and voltage-balancing problem). This topology requires fewer components as compared to existing inverters (such as; diode clamped (DCMLI), flying capacitor (FCMLI), cascaded h-bridge (CHBMLI)) and requires fewer carrier signals for PWM implementation and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage level. The main purpose of our dissertation is to study the different modulation techniques and compare them with each other analyzing their advantages and disadvantages and to analysis that series parallel switching multilevel inverter topology is better than conventional multilevel inverters topology in terms of their number of components and THD.

This dissertation also presents information about several multilevel inverter topologies, such as the DCMLI, FCMLI and the CHBMLI. These multilevel inverters will also be compared with two-level inverters in simulations to investigate the advantages of using multilevel inverters. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed. Sine-triangle carrier modulation is identified as the most promising technique for multilevel inverter.

A single-phase 11-level, 15-level & 19-level multilevel inverter is simulated with the help of MATLAB/SIMULINK R2013a software version and the harmonic spectrum is also calculated.

Key words, MLI Simulation SPSMLI Method THD , comparison between - 11 - level, 15 - level and, 19 - level multi - level inverter

SIMULATION RESULT

1.1. INTRODUCTION

In this chapter performance of the proposed SPSMLI are studied. The MATLAB-simulink is used to simulate 11, 15 and 19 level inverters. One of the key features is that it allows the user to simulate the design over a specified period of time.

1.2. SIMULATION OF 11 LEVEL SERIES PARALLEL SWITCHING MULTILEVEL INVERTER

Figure 1.1 represents the model of an 11 level Series Parallel Switching Multilevel inverter.

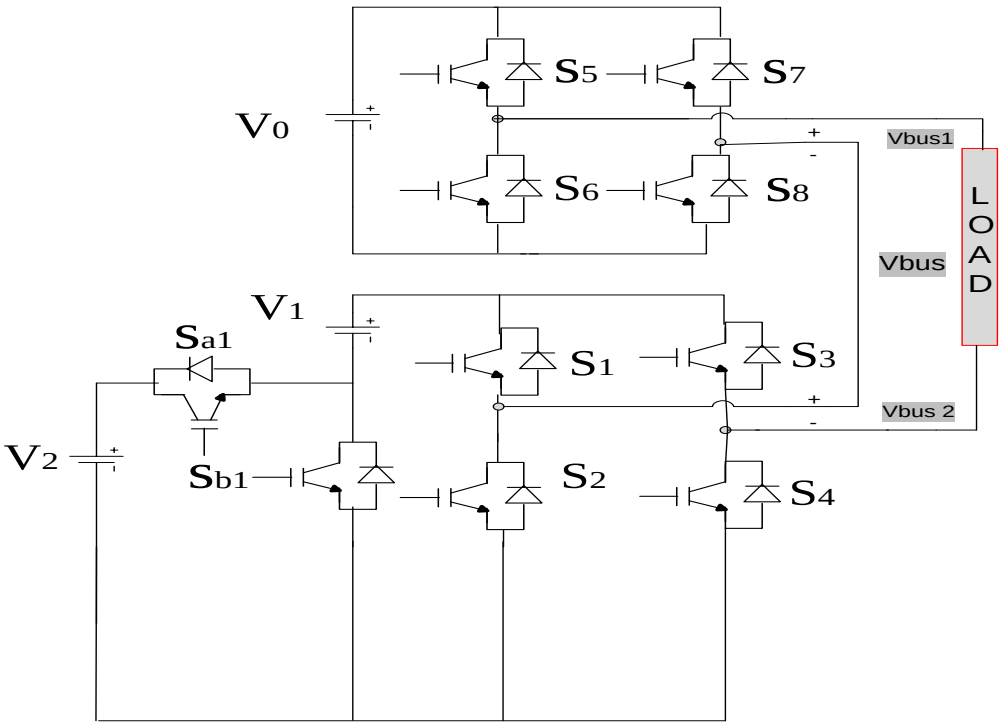


Figure 1.1 11 level series parallel switching multilevel inverter

1.2. Simulation Results

Figures1 1.2 - 5.7 shows the phase voltage, & Figures 5.8 – 5.13 THD of an 11 level inverter by the using of different PWM techniques at a modulation index of 0.9. Table 5.1 represents the THD at different modulation indices and also shows the THD value changes according to the modulation index.

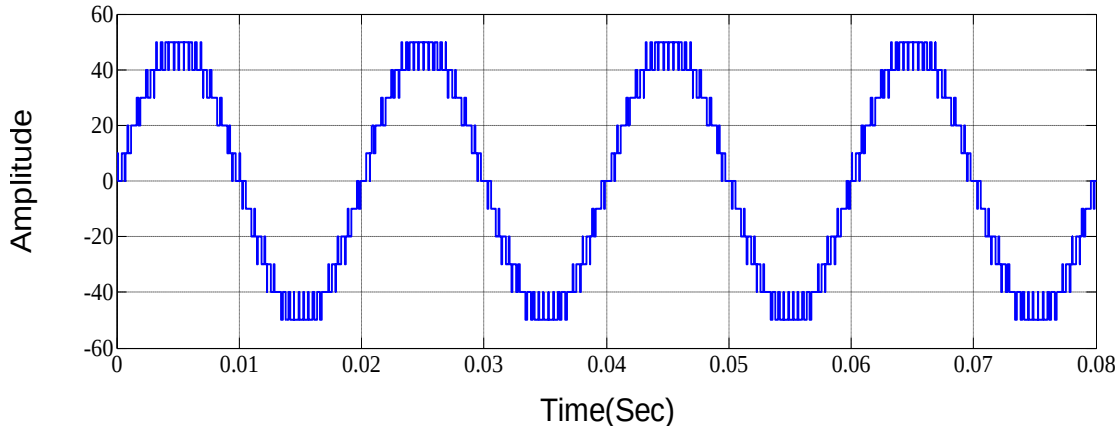


Figure 1.2 Simulated 11 level output voltage generated by PD PWM technique for RL-load

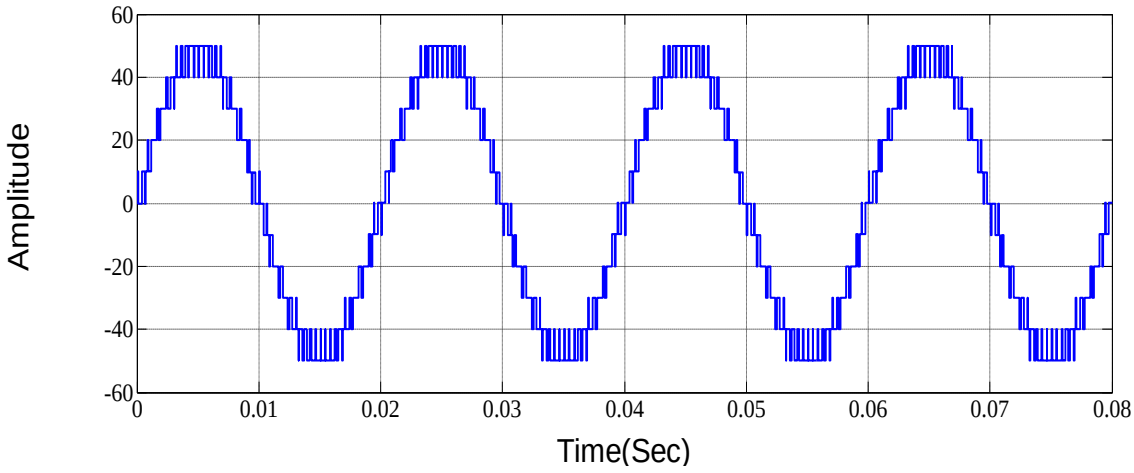


Figure 1.3 Simulated 11 level output voltage generated by POD PWM technique for RL-load

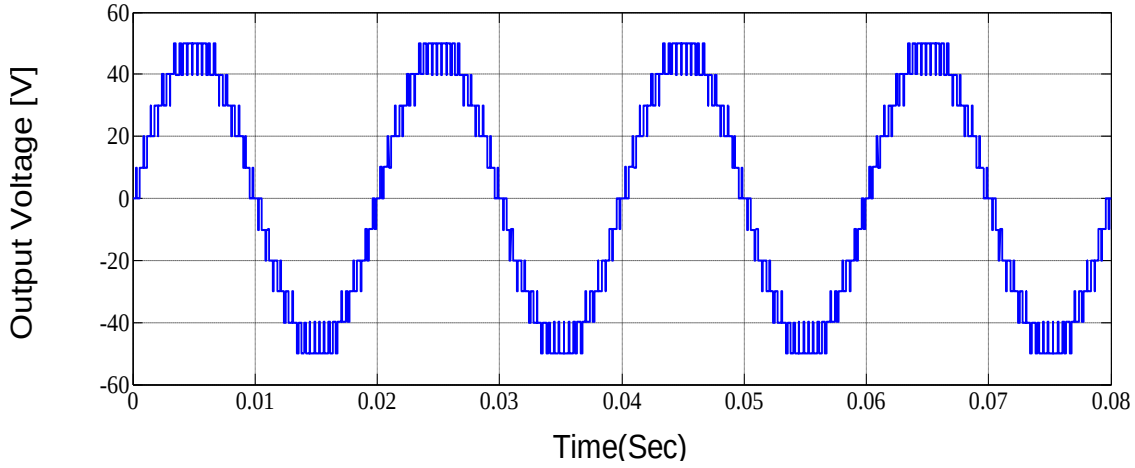


Figure 1.4 Simulated 11 level output voltage generated by APOD PWM technique for RL load

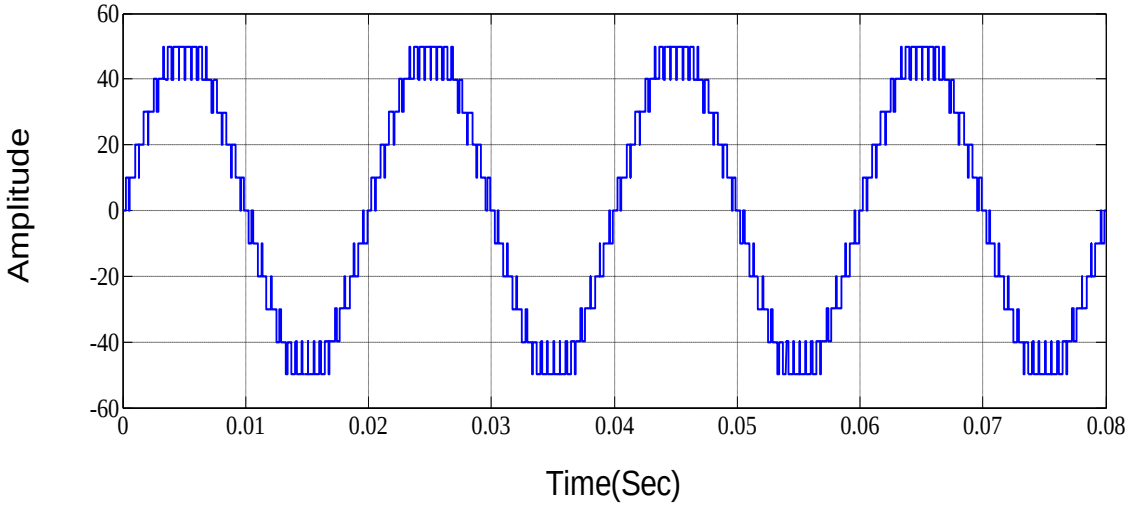


Figure 1.5 Simulated 11 level output voltage generated by PS PWM technique for RL-load

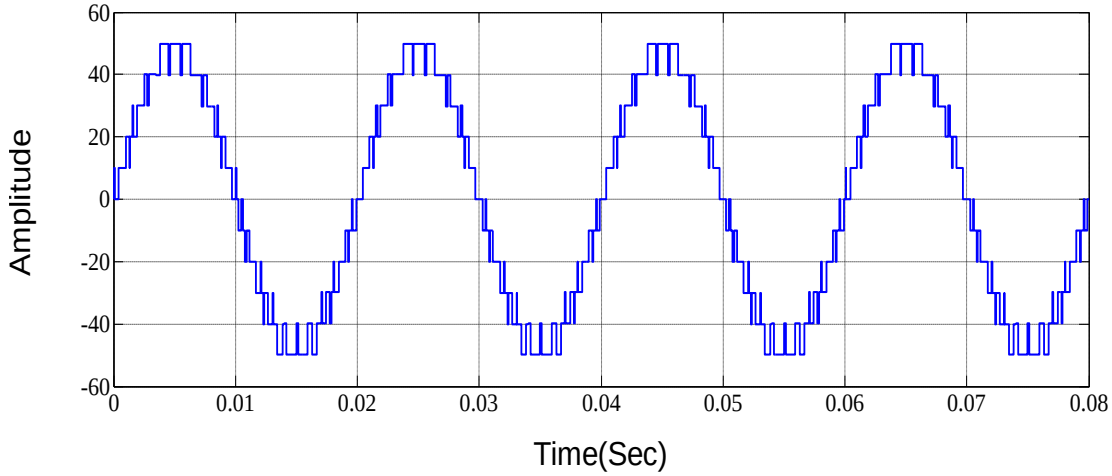


Figure 1.6 Simulated 11 level output voltage generated by VF PWM technique for RL-Load

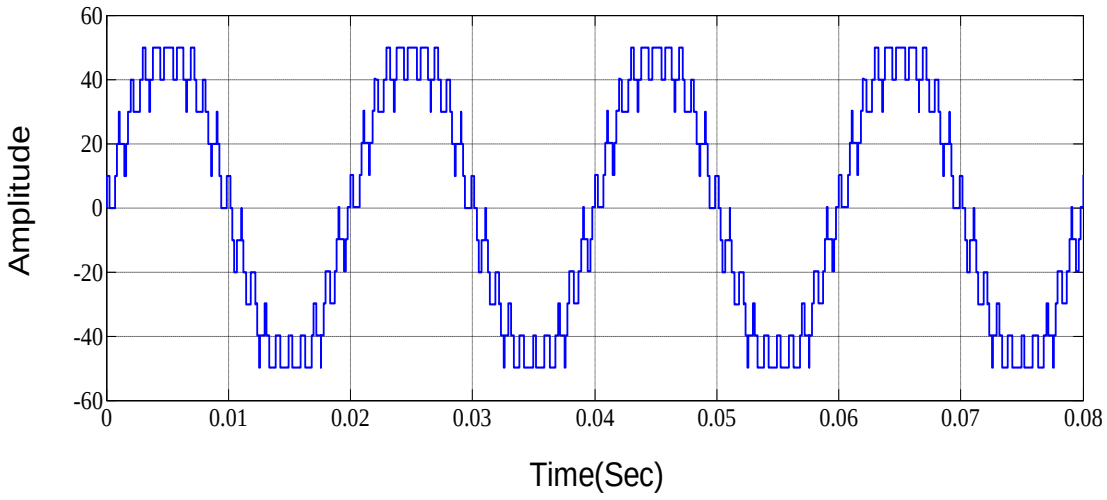


Figure 1.7 Simulated 11 level output voltage generated by CO PWM technique for RL-Load

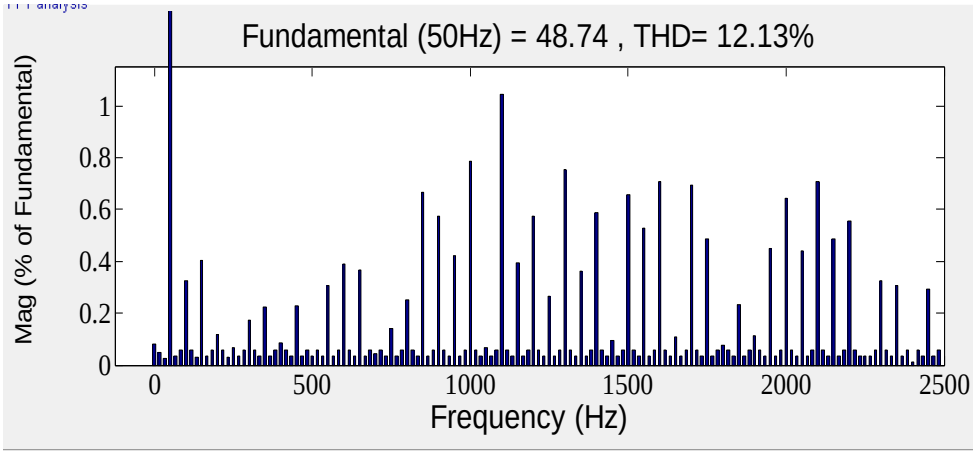


Figure 1.8 Harmonic spectrum of output of PD PWM technique at modulation index = 0.9

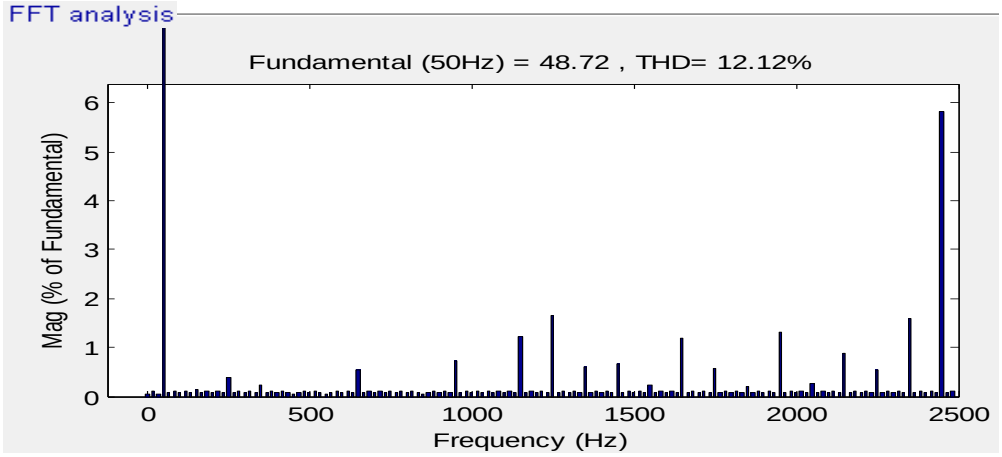
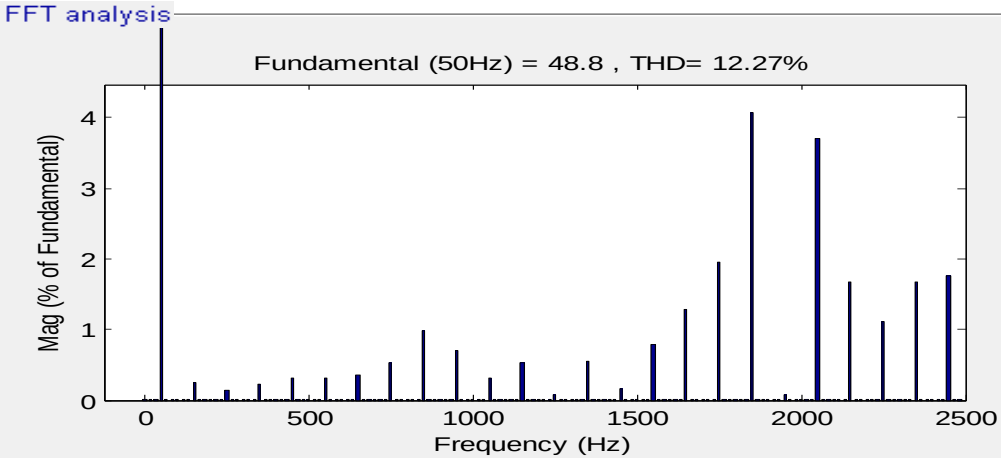


Figure 1.9 Harmonic spectrum of output of POD PWM technique at modulation index = 0.9



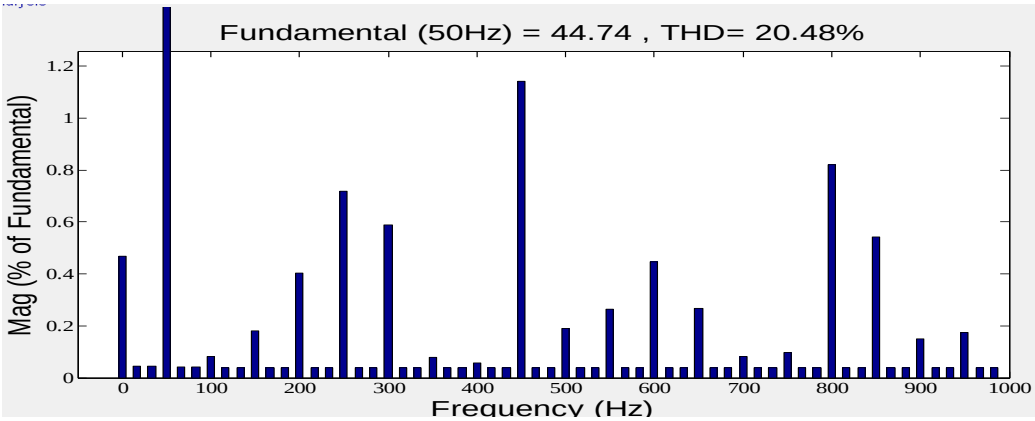


Figure 1.10 Harmonic spectrum of output of CO PWM technique at modulationindex = 0.9

Table 1.1 Modulation Index Vs THD in an 11 level Inverter

Modulation Index	PD PWM % THD	POD PWM % THD	APOD PWM % THD
0.9	12.13	12.12	12.27
0.8	12.30	12.37	12.33
0.7	12.97	12.65	12.87
0.6	13.04	13.08	13.05

2.1 CONCLUSION

This dissertation has provided a brief summary of multilevel inverter circuit topologies (11 level, 15 level and 19 level) and their analysis.

Each MLI has its own mixture of advantages and disadvantages and for any one particular application, one topology will be more appropriate than the others. Often, topologies are chosen based on what has gone before, even if that topology may not be the best choice for the application. The advantages of the body of research and familiarity within the engineering community may outweigh other technical disadvantages. Multilevel converters can achieve an effective increase in overall switch frequency through the cancellation of the lowest order switch frequency terms. As discussed in Chapter 3, among the multilevel converter topologies, the series parallel switching multilevel inverter topology is the most promising alternative for industry application.

In the fourth chapter, we have discussed different types of carrier based PWM modulation techniques. There are many modulation techniques for multi level inverters. But carrier based modulation technique is easy and efficient. The PWM output spectra were calculated from basic operation simulated using MATLAB.

The simulation results for 11 level, 15 level and 19 level series parallel switching multilevel inverters are presented in chapter 5. Their harmonic analysis is also discussed. THD of the three series parallel switching multilevel inverters have been calculated at different modulation index.

2.2 FUTURE WORK

With the help of series-parallel switching multilevel inverter topology we will increase the voltage levels with less number of power switches, capacitors and diodes. This topology is compare with the DCMLI, CHBMLI and FCMLI and then fed with the induction motor drives.

3. REFERENCES

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