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Performance Analysis of a New Single Phase Single Source 7-Level Inverter Topology Using Different SPWM Techniques

Liju Shaji
M.E student, Dept of EE,
Madhav Institute of Technology & Science,
Gwalior, India.
shaji.liju87@gmail.com

Praveen Bansal
Assistant Proffesor, Dept of EE
Madhav Institute of Technology & Science,
Gwalior, India.
pbansal444@gmail.com

Dr.Vijay Bhuria
Assistant Proffesor, Dept of EE
Madhav Institute of Technology & Science,
Gwalior, India.
vijay.bhuria@mitsgwalior.in

***Abstract* — This paper deals with the performance analysis of a new 7-level switched capacitor based multilevel inverter (MLI) when driven using various PWM techniques. This inverter topology, unlike the conventional switched capacitor topology is a single stage inverter employing only one dc source. The inverter topology under analysis consists of three H-bridge which are connected via two bidirectional voltage blocking switches. The new MLI topology analyzed in this paper use low voltage rating switches i.e., the switches in new MLI topology have to block low voltage levels when compared to its conventional counterpart. Moreover, the new MLI topology analyzed in this paper produce a 7-level waveform with a voltage boosting factor of three with the use of a single voltage source. The total harmonic distortion (THD) of the new 7-level switched capacitor MLI topology is calculated by using different multi carrier based PWM techniques like Phase disposition (PDPWM), Phase Opposition Disposition (PODPWM), Alternate Phase Opposition Disposition (APODPWM), Carrier Overlap (COPWM), Phase Shift (PSPWM).**

Keywords—Multilevel inverter, Boosting-factor, Switched-Capacitor (SC), PDPWM, PODPWM, APODPWM, VFPWM, COPWM, PSPWM

I. INTRODUCTION

Over the period of few decades, multilevel inverter has become a key technology for high-quality high-power DC-AC conversion. With the ever-increasing use of non-conventional sources of energy such as fuel cells, photovoltaic cells and with the development of HVDC transmission system, the need for multilevel inverter has exponentially increased. Above all, the use of two-level inverter produces a highly polluted output voltage waveform when compared to the multilevel inverter topologies.

The traditional multilevel inverter is basically categorized into three types: neutral point clamped [1], flying capacitor [2] and the cascaded H-bridge [3], the role of these multilevel inverters has been very vital in various mid-range and high-end industrial applications. These multilevel inverters possess an important limitation i.e., as the output levels increases the switch count of these multilevel inverter also increases. As a result, a number of new multilevel topologies with reduced device count have been described in [4].However, these reduced count multilevel inverter have other limitations like need of multiple isolated DC source and high voltage stress across the semiconductor switch at the polarity generation side. Also, attention should be directed to the fact that the voltage boosting factor for these multilevel inverters is confined to only one. One such topology discussed in [4] was the Cascaded Half-Bridge based Multilevel DC Link inverter. It consists of cascaded half bridge cells with each cell comprising of a voltage source of its own. The cascaded half bridge cells works as the level generation stage producing positive level voltages and the H-bridge side makes up the polarity generation side, producing the required bipolar waveform. T-inverter was another such topology discussed in [4], which was again a two-stage topology having reduced device count. When compared to a conventional H-bridge topology these inverters can reduce device count as number of voltage level increases. But they suffered from a major limitation of low voltage boosting factor

To improve the low voltage boosting factor of the above said topologies, recently, switched capacitor has been employed in many multilevel inverter topologies to enhance the voltage boosting factor [5] [6] [7]. But the enhanced voltage boosting factor of these topologies has been greatly over shadowed by the fact that the switches in the polarity generation side of these multilevel inverters has to block voltages as high as the peak output voltage of inverter.

There are different type of modulation techniques which are employed in an inverter to achieve simple implementation as well as improved inverter efficiency. These modulation techniques are further classified into two major groups, namely; carrier based modulation and carrier less modulation technique. Carrier based modulation technique consists of different PWM technique like Sinusoidal PWM (SPWM), Modified PWM (MPWM), Space Vector PWM (SVPWM), 3rd Harmonic Injected PWM. Out of these PWM techniques SPWM is the most commonly used PWM technique [8] [9]. In this paper different SPWM techniques such as PD, POD, APOD, PS, CO PWM techniques have been employed to evaluate the performance of the new MLI topology.

The topology under analysis in this paper has two main merits, firstly, it has a triple voltage boosting factor, and secondly, the voltage appearing across each power semiconductor switch is limited to a low value equal to V_{dc}. This paper gives a comprehensive evaluation of the new MLI topology when driven using different SPWM and then

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