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Various modulation techniques in symmetrical multilevel inverters

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2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS)
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A Multilevel Inverter Topology using Reverse-Connected Voltage Sources

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***Abstract*: This paper presents a new single phase H-bridge multilevel inverter topology using reverse- connected voltage source along with a different pulse width modulation (PWM) strategy, to extract a variable frequency variable amplitude output voltage. It involves the use of reduced number of switching devices for a specific number of output voltage levels in comparison with conventional MLIs. Using this configuration, the total harmonic distortion is reduced as total harmonic distortion plays an important role in medium voltage and high power applications for better operation so here with new proposed topology the total harmonic distortion diminishes. In this paper simulation results of the proposed multilevel inverter for a single-phase 7- level multilevel inverter are presented and the total harmonic distortions results of 7, 9, 11-level with different modulation index are shown.**

Keywords — H-bridge multilevel inverter, Total harmonic Distortion (THD), Multicarrier pulse width modulation (MC-PWM)

I. INTRODUCTION

The Multilevel inverter is extended version of an inverter. The Multilevel inverter emerged in the industrial environment in during 1975 [1], because of increasing the necessity of better system efficiency and good quality of power in the industry. In a competitive and growing world with the demand of higher voltage and power with good quality in industry, the necessity of multilevel inverter increases, the multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulting in lower harmonics.

As compared with the two level inverter structure the multilevel inverter provides the AC voltage nearer to sinusoidal voltage with the lower harmonic content in the output voltage waveform, reduced dv/dt stress across the switch, lower switching losses i.e. improved efficiency and lower EMI and filter size is also reduced [2-5].

Multilevel inverter also have some disadvantages i.e. large number of power semiconductor switches required and each switch requires respective gate driver circuit which makes the configuration complex and system becomes costly. So here this is very important to compromise between cost and voltage quality. The conventional topologies for multilevel inverter are cascade H-bridge (CHBMLI), diode clamped (DCMLI) and flying capacitor (FCMLI).

Cascade H- bridge has the simplest construction among all three multilevel inverter topology, as it requires less number of components [6]. The cascade H- bridge multilevel inverter consists of a number of n H-bridge inverter cell. In each cell the four main switch and one separate dc voltage source is used [7]. As these cells are connected in series the level is easily scaled without any complexity in the circuit here n = 1 H bridge. For N level voltage generation the cascade H-bridge MLI uses 2(N-1) Main switch and (N-1)/2 voltage sources, Then total number of component used is 5(N-1)/2.

For diode Clamped multilevel inverter the clamping diode is used to transfer a limited amount of voltage [8]. For N level voltage generation 2(N-1) switching devices which are connected in series, (N-1)*(N-2) clamping diode, (N-1) dc link capacitor to divide the dc link into different voltage level and one dc source is required, Then total number of component required is N^2.the maximum output voltage is half of input dc voltage, this is a big drawback of diode clamped multilevel inverter but this type of inverter provides high efficiency because of fundamental frequency used for all switching devices.

Flying capacitor multilevel inverter was first introduced in 1992. This is almost similar in construction wise to diode clamped multilevel inverter.it uses capacitors instead of clamping diode. For N level flying capacitor 2(N-1) switching devices, (N-1)*(N-2)/2 clamping capacitor, (N-1) dc link capacitor and 1 dc voltage source is required so total number of component $(N^2+3N-2)/2$ required, where N is total number of level. In flying capacitor MLI the components required are less in comparison to diode clamped MLI [9], but efficiency is less because the flying-capacitor MLI uses high switching frequency, so switching losses will takes place.

This paper uses Cascade H–bridge multilevel inverter (CHBMLI) connected with the reverse voltage sources [10]. This is simple configuration to obtain higher voltage levels, as voltage level increases, a reverse voltage source is connected with this structure. For Harmonic reduction in output voltage waveform, this paper highlights Multi carrier pulse width modulation based cascade H bridge multilevel inverter.

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II. PROPOSED MLI TOPOLOGY

The proposed multilevel inverter topology uses one cell of H-bridge with four main switches and one voltage source vs. this one cell of H- bridge is connected with complementary switches (S5 to Sn+3) and reverse connected voltage sources (V1 to Vn) . The voltage sources Vs and V1 to Vn are of same magnitude and used for level addition and subtraction, and complementary switches (S5 to Sn+3) are used for voltage cascading and provides a bypass when particular voltage is not consider [10].

This reverse connected multilevel inverter topology starts with 5 level. To extract the output voltage of N level, the switches used are N+3.In figure 1 the proposed topology shown and The 7 level proposed multilevel inverter topology shown in figure 2. For example, a 7 level Proposed MLI topology requires 10 switches. The switches used depends upon the switching frequency and switches are switched at carrier frequency [10]. The switches are ON accordingly to voltage level. The switching scheme is shown in table 1. To generate +3Vdc the switch S3, S4, S6, S8, S10 are on and rest are off as shown in operating modes figure 6.(f).

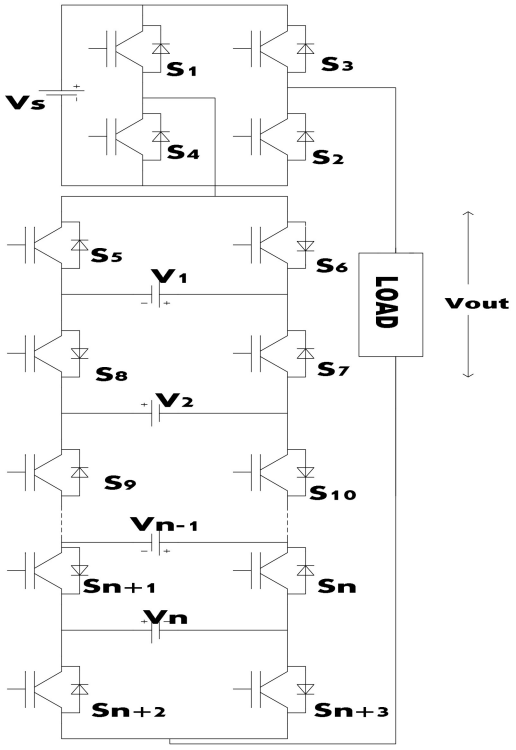


Fig 1: Proposed Topology (Auxiliary Reverse connected Voltage sources)

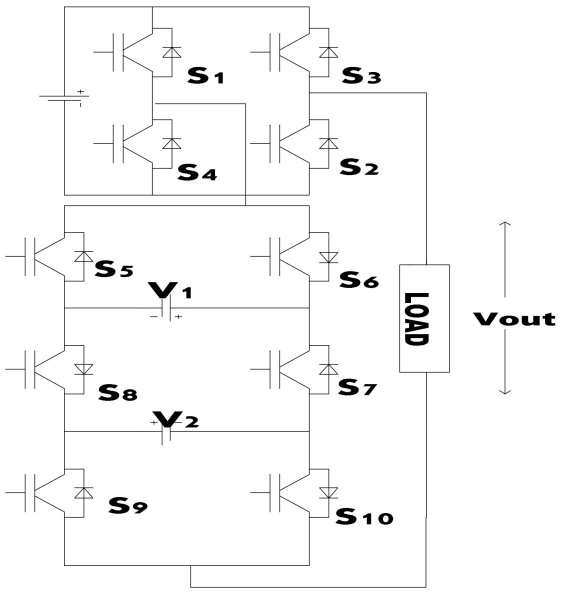
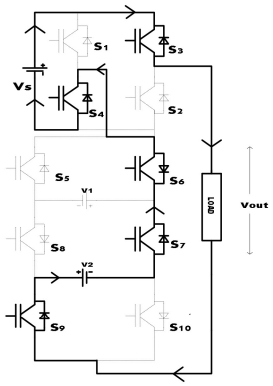


Fig.2: Proposed Topology 7- Level MLI

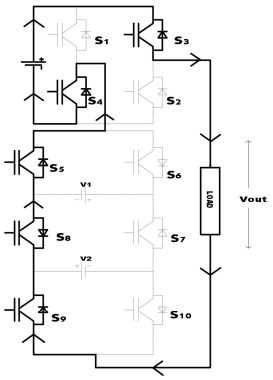
TABLE 1: SWITCHING SCHEME OF PROPOSED 7- LEVEL MLI

OUTPUT VOLTAGE	SWITCHING SCHEME									
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
+3Vdc	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON
+2Vdc	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF
+Vdc	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF
0Vdc	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF
-Vdc	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON
-2Vdc	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
-3Vdc	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF

III. OPERATING MODES OF PROPOSED TOPOLOGY



Level 0
Fig. (a)



Level +1
Fig. (b)

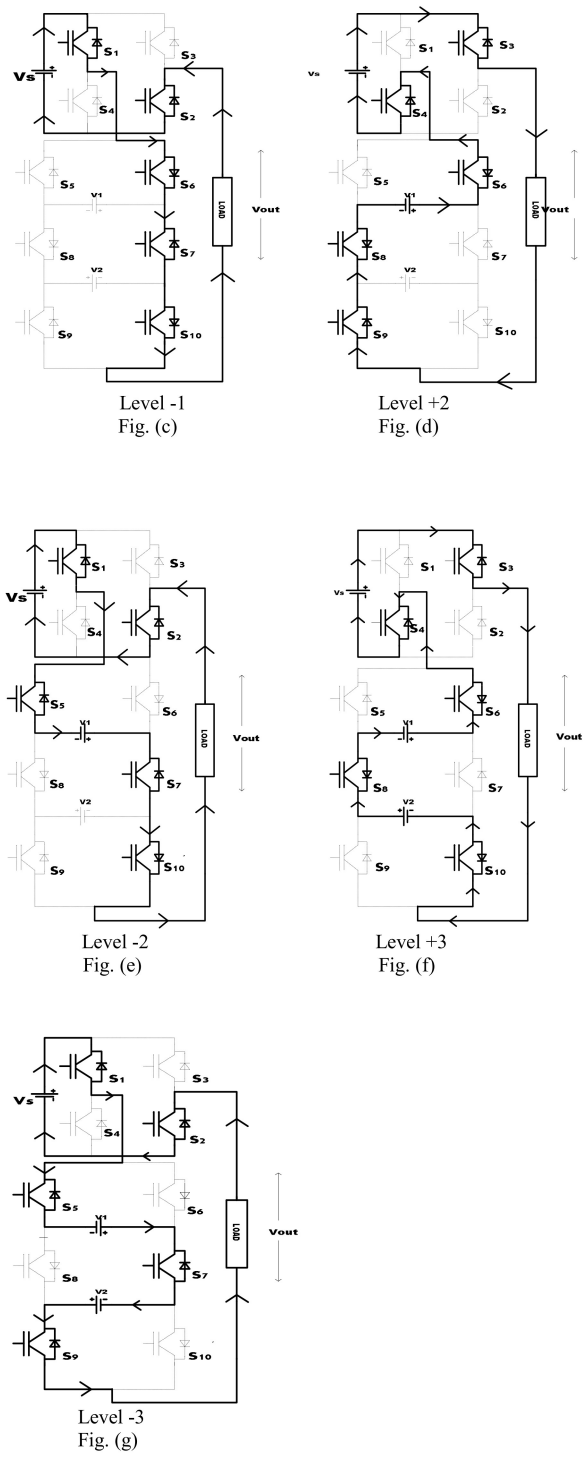


Fig.3: Fig (a), Fig (b), Fig (c), Fig (d), Fig (e), Fig (f) and Fig (g) are operating modes of 7- Level MLI.

TABLE 2: DETAILED COMPARISON OF POWER COMPONENT BETWEEN CONVENTIONAL AND PROPOSED TOPOLOGIES

MULTILEVEL INVERTER STRUCTURE COMPONENTS	CASCADE H- BRIDGE	DIODE CLAMPED	FLYING CAPACITOR	PROPOSED TOPOLOGY
MAIN SWITCH	2(N-1)	2(N-1)	2(N-1)	N+3
CLAMPING DIODES	-	(N-1)*(N-2)	-	-
DC SPLIT CAPACITOR	-	(N-1)	(N-1)	-
CLAMPING CAPACITORS	-	-	$\frac{(N-1)*(N-2)}{2}$	-
DC SOURCES	$\frac{(N-1)}{2}$	1	1	$\frac{(N-1)}{2}$
TOTAL	$\frac{5(N-1)}{2}$	N^2	$\frac{N^2+3N-2}{2}$	$\frac{3N+5}{2}$

IV. CONTROL AND MODULATION STRATEGIES IN PROPOSED TOPOLOGY

In the modulation techniques Reference wave (modulating wave) is compared with carrier wave [11]. For an N level inverter (N-1) carriers are employed. The reference signal is a sinusoid of frequency 50 Hz and the carrier wave has a higher frequency compared with reference wave. At every instant each carrier is compared with reference signal, here condition is applied as if reference wave is greater than carrier wave, the comparison gives result one and otherwise zero, these results are added and which gives the voltage level with different modulation index. Modulation index or modulation ratio play an important role, as modulation index varies with the total harmonic distortion (THD). Amplitude modulation index is the ratio of amplitude of reference signal to peak to peak amplitude of carrier.

In this paper Multi carrier pulse width modulation (MC-PWM) technique and Hybrid Modulation Techniques are used. These Modulation Techniques are as-

a) Phase Disposition PWM (PDPWM)
b) Phase Opposition Disposition PWM (PODPWM)
c) Alternative Phase apposition Disposition PWM (APODPWM)
d) Inverted Sine Carrier PWM (ISCPWM)
e) Variable Frequency Inverted Sine Carrier PWM (VFISCPWM).

Here first three PDPWM, PODPWM, APODPWM are the multicarrier pulse width modulation technique and last two ISCPWM and VFISCPWM are hybrid modulation technique.

a) Phase Disposition PWM (PDPWM) Method:

The phase Disposition Techniques has all (N-1) carrier waveform in phase with same frequency and amplitude above

and below the zero reference which is placed in the middle of carrier set [12].in the figure 4. For 7 level inverter the (7-1) = 6 carrier are shown.

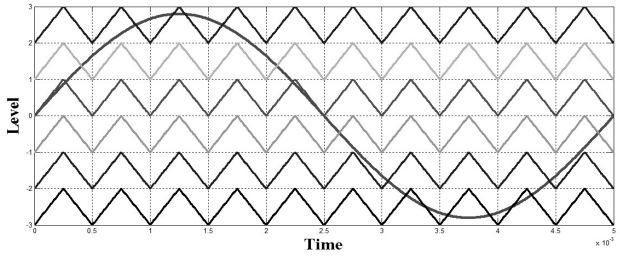


Fig.4: Carrier Arrangement for PD PWM technique

b) Phase Opposition Disposition PWM (PODPWM) Method:

With the POD technique the carrier waveform above and below zero reference value are in phase .however they are phase shifted by 180 degree between the carrier Waveform above and below Zero [13].

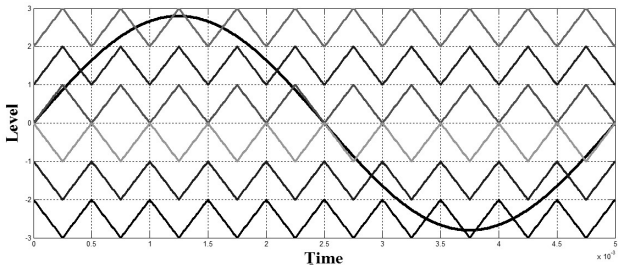


Fig. 5 Carrier arrangement for POD PWM technique

c) Alternative Phase Opposition Disposition PWM (APODPWM) Method:

This Technique also have the zero reference is placed in middle of carrier set. The above and below the zero reference all (N-1) carrier wave have same amplitude and frequency but out of phase with its neighboring carrier wave by 180° [13]. The output voltage of a seven level inverter which Uses APOD PWM Control Techniques is as follows in fig. 6.

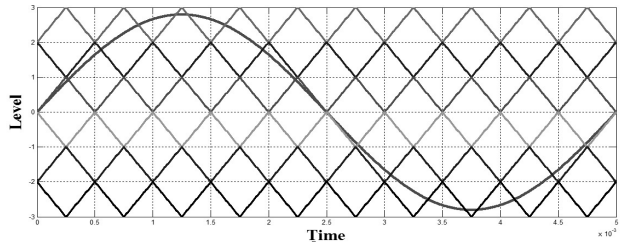


Fig.6: Carrier arrangement for APOD PWM technique

d) Inverted Sine Carrier PWM (ISCPWM) :

This Control Method Replace the Conventional Triangular based Carrier waveform by inverted sine wave which has the combine advantage of inverted sine and constant or variable frequency carrier signals. The inverted sine carrier PWM (ISCPWM) Techniques uses the Sine wave as Reference signal and carrier signal is an inverted sine carrier with high frequency. This combination of reference and carrier signal with different modulation index produces output voltage with low harmonic distortion.

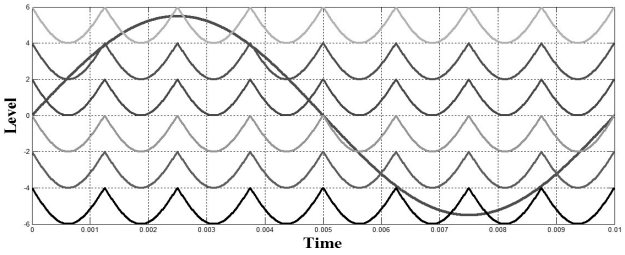


Fig.7: Carrier Arrangement for ISCPWM technique

e) Variable Frequency inverted sine carrier PWM (VFISCPWM) :

In variable frequency inverted sine carrier technique sine wave as a reference signal and carrier signals are inverted sine signal with variable frequency.

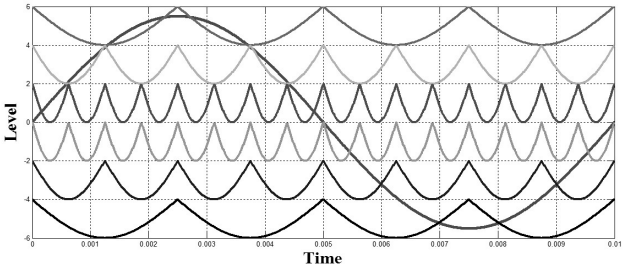


Fig.8: Carrier Arrangement for VFISCPWM technique

V. SIMULATION RESULT

The proposed multilevel inverter topology is simulated in MATLAB/SIMULINK R2010b with source voltage V_s = 10V, V_1 to V_n = 10 V, switching frequency of carrier 2000 Hz, R= 10 Ω. In this paper five modulation techniques is used to control the proposed multilevel inverter.

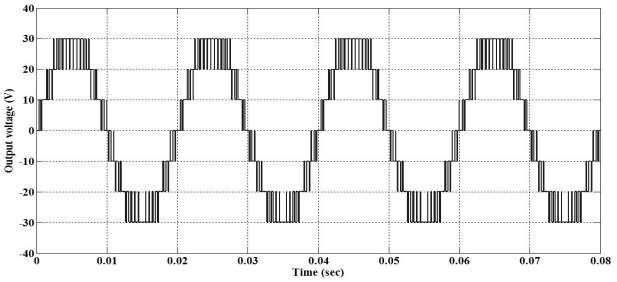


Fig 9: Output voltage waveform of 7- level proposed MLI

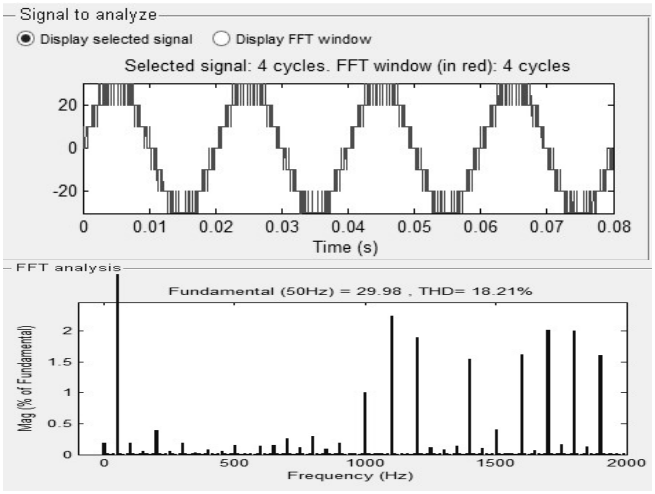


Fig.10: THD of 7- Level MLI with PD modulation Scheme and modulation index 1

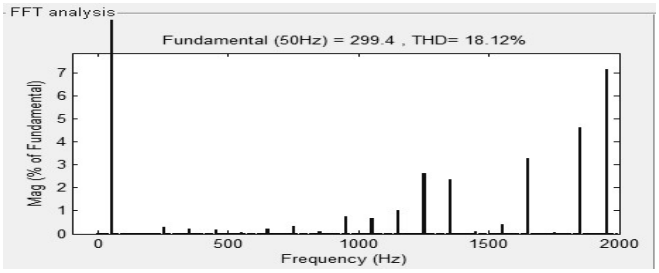


Fig.11: THD of 7- Level MLI with POD modulation scheme and modulation index 1

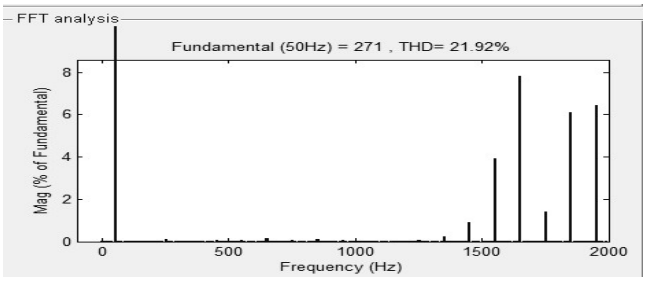


Fig.12: THD of 7- Level MLI with APOD modulation scheme and modulation index 0.9

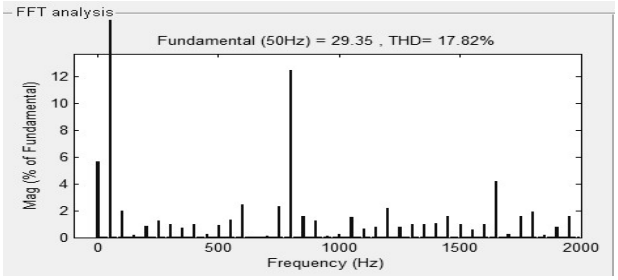


Fig.13: THD of 7- Level MLI with ISC modulation scheme and modulation index 1

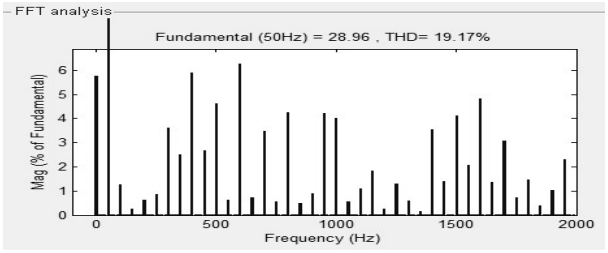


Fig.14: THD of 7-level MLI with VFISC Modulation scheme and modulation index 1

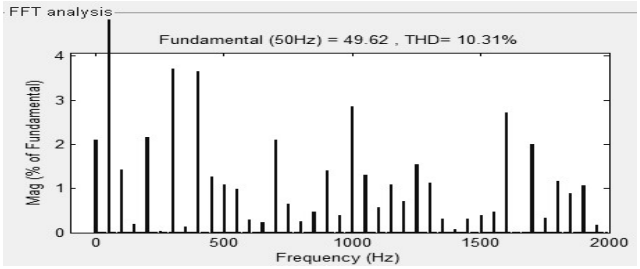


Fig.15: THD of 11-level MLI with VFISC Modulation scheme and modulation index 1

TABLE.3: COMPARISON OF DIFFERENT MODULATION TECHNIQUE RESULT

Level	Modulation Index	Modulation Techniques				
		PD	POD	APOD	ISC	VFISC
7 level	1	18.21	18.12	18.34	17.82	19.17
	0.9	22.38	22.05	21.92	20.30	20.02
	0.8	24.33	24.00	24.12	23.60	24.39
9 level	1	13.74	13.44	14.13	14.27	12.42
	0.9	16.79	16.77	16.82	18.16	16.84
	0.8	17.21	16.97	17.13	17.40	18.04
11 Level	1	11.05	10.72	11.08	17.54	10.31
	0.9	13.03	12.97	12.00	14.02	13.66
	0.8	13.76	13.48	13.38	14.27	14.61

VI. CONCLUSION

In this paper a new multilevel inverter topology, which has superior performance over conventional topologies, is introduced. This has provided improved output waveforms and lower THD as seen in Table 3 with different modulation schemes and different modulation indexes. For 11 level, THD is 10.31% with modulation index 1 using variable frequency inverted sine carrier modulation scheme which is less in compared to conventional topologies result. As seen in Table 2 the proposed topology required less switches as compared to conventional topologies [14-16], so that cost, complexity and controlling (as gate driver circuit required less) reduced and

reliability and efficiency improved. The proposed topology and fundamental switching scheme results in a near-sinusoidal Waveform. As a result, a significant reduction of output voltage THD is obtained. The proposed multilevel inverter has many merits such as ability to synthesize waveforms with better harmonic spectrum, reduced THD and dv/dt stress.

VII. Acknowledgement

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