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Various Modulation Techniques In Symmetrical Multilevel Inverters

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Abstract— Multilevel inverters are the versatile tool for running highly rated machines. However it can work satisfactorily for medium and low rating machines, concerning to their advantages like lower EMI, suppressed harmonic distortion and higher DC-link voltages it is manifolds better to a conventional two level inverter. Their main drawback is complexity, Because it requires large number of batteries and switches. In this paper a symmetrical inverter topology for generation of nine levels of output voltage with reduced number of switches is presented. This technology employs lesser circuit elements compared to other techniques hence significantly reduces the complexity. The performance of present technology is executed by MATLAB/SIMULINK platform and the results showing the operation of the present topology as multilevel inverter is presented.

Keywords— Multilevel inverter (MLI), Multi-level DC-link inverter (MLDCLI),Pulse Width Modulation (PWM), THD.

1. INTRODUCTION

In recent years, multilevel inverter has occupied a large part of the industry, due to use in high power and high voltage application [7]. The word 'multi-level inverter' was first introduced in year 1970s and 1980s. The fundamental unit of a multilevel inverter is called three level, it is similar to a square waveform [3]. Multilevel inverter has certain advantages over two level inverters such as, low switching frequency hence reduction in switching losses, lower harmonic, low common mode voltage. An MLI generates a stepped waveform which looks like a sinusoidal, alternately it generates an increasing and decreasing staircase waveforms by increasing the voltage levels. Staircase waveform so generated will tend towards pure sinusoidal which in turn leads to require more gate driver circuits. Different PWM techniques are used to control output voltage waveform within multilevel inverter [1].

Power electronic inverter are used in adjustable speed ac drive, induction heating, stand by air-craft power supplies, ups (uninterruptable power supplies) for computer, HVDC transmission lines etc [2]. MLI are preferred for medium and high power system like static reactive power compensation. MLI reduced total harmonic distortion content in output side. Cause of technical and economical barrier like that cost of drive and protection, stable dc supply voltage and packing, the number of inverter to be limited.

Several MLI has been classified as Diode-clamped converter, Capacitor-clamped converter [4]; cascaded converter .MLI has some disadvantage that they require large number of power semiconductor switches [5]. Switch related to gate drive circuit, so the overall system is complex and more expensive. This type of inverter is inconveniences for balancing capacitor voltage [6]. In case of series parallel dc-link inverter reduced distortion of sinusoidal output voltage with less number of sources capacitor and power switches. In this paper a new topology of symmetrical multi level inverter is introduced which require for reduced distortion of sinusoidal voltage and less number of power switches. In this topology H-bridge is used with bidirectional power flow. By increasing number of level proposed 9-level MLI can be achieved. Simulation result of 9-level can be obtained by MATLAB/ SIMULINK software.

2. SYMMETRICAL MULTILEVEL INVERTER

The basic unit for a proposed symmetric multilevel inverter is shown in Fig.1 In this circuit, when the switch "S" is turned off, the current flows from the diode, but when the switch "S" is turned on, the diode is reverse biased and the current flows through dc voltage source (V) which is connected in series with switch. Hence, using this method the output voltage is controlled. This method is the base of the proposed multilevel inverter and the basic unit generates five levels in output voltage and TABLE 1 shows the value of output voltages (V_o) for different states of switches T_1,T_2,T_3,T_4 and S.

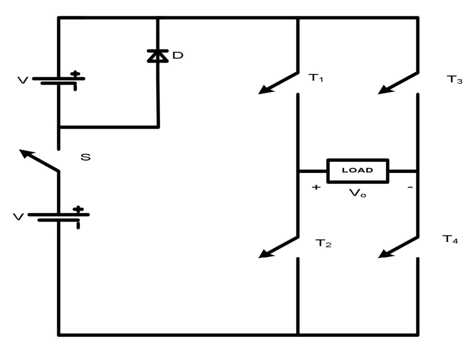

Fig. 1 Basic unit

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TABLE 1
Different Switching States For basic unit

OUTPUT VOLTAGE	SWITCHING STATES				
	S	T_1	T_2	T_3	T_4
+2V	ON	ON	OFF	OFF	ON
+V	OFF	ON	OFF	OFF	ON
0V	OFF	ON	OFF	ON	OFF
-V	OFF	OFF	ON	ON	OFF
-2V	ON	OFF	ON	ON	OFF

Fig. 2 shows the extended circuit of the 9-level inverter. The magnitude of the DC voltage sources are equal (100V). Therefore the structure is called symmetric multilevel inverter, which consist of a basic unit and a full bridge converter.
TABLE 2 shows the value of output voltages (V_o) for the different states of S_1,S_2,S_3,S_4,S_5,S_6 and S_7 switches. Note that there are several switching states to obtain the zero voltage but only one of them is shown in the TABLE 2.

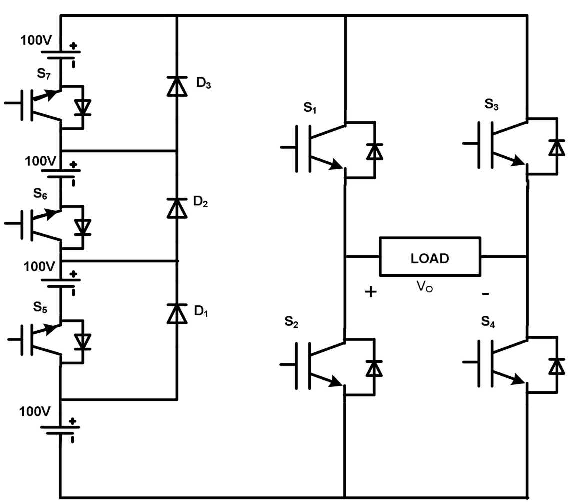

Fig. 2 symmetric multilevel inverter

The number of output voltage levels and the total number of switches in the recommended symmetric multilevel inverter are obtained as follows, respectively

$$N_{level} = 2n + 3 \quad (1)$$
$$N_{IGBT} = n + 4 \quad (2)$$

where n represents the number of IGBTs in the symmetric basic unit structure. In this topology, the maximum output voltage (Vo,max) is

$$V_o, max = (n+1)\times V \quad (3)$$

Using (1) and (2), we have

$$N_{level} = 2N_{IGBT} - 5 \quad (4)$$

TABLE 2
Switching States For 9-level Symmetrical multilevel inverter

OUTPUT VOLTAGE	SWITCHING STATES						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
+400V	ON	OFF	OFF	ON	ON	ON	ON
+300V	ON	OFF	OFF	ON	ON	ON	OFF
+200V	ON	OFF	OFF	ON	ON	OFF	OFF
+100V	ON	OFF	OFF	ON	OFF	OFF	OFF
0V	ON	OFF	ON	OFF	OFF	OFF	OFF
-100V	OFF	ON	ON	OFF	OFF	OFF	OFF
-200V	OFF	ON	OFF	OFF	ON	OFF	OFF
-300V	OFF	ON	ON	OFF	ON	ON	OFF
-400V	OFF	ON	ON	OFF	ON	ON	ON

3. OPERATING MODES

Various operating modes to obtain different voltage levels are shown in the following figures.

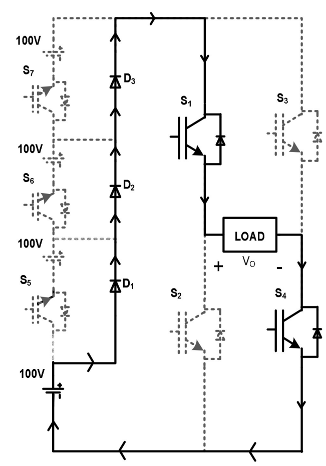

Fig. 3 (+100V)

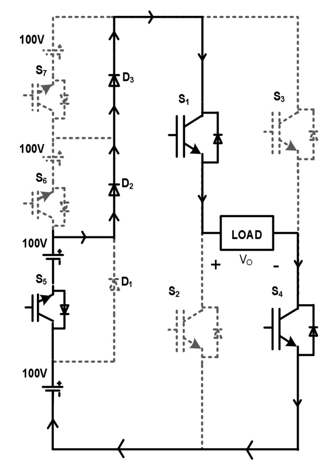

Fig. 4 (+200V)

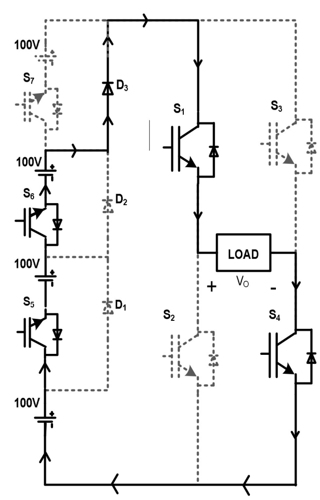

Fig. 5 (+300V)

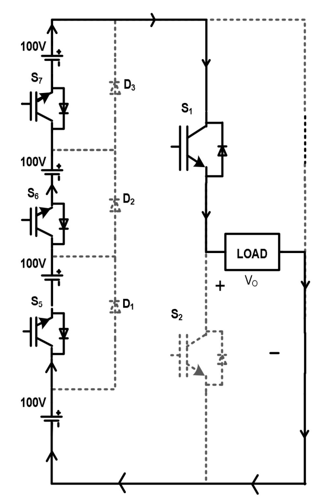

Fig. 6 (+400V)

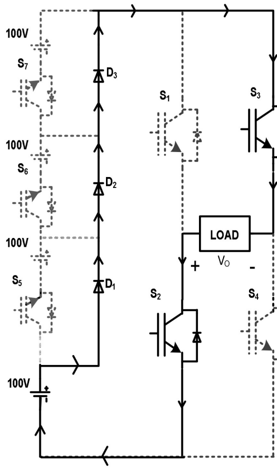

Fig. 7 (-100V)

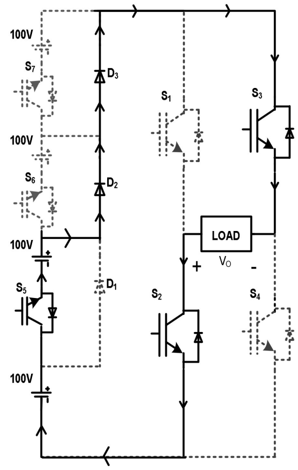

Fig. 8 (-200V)

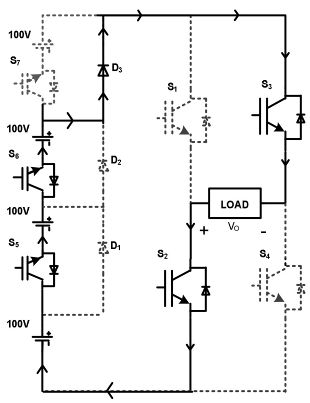

Fig. 9 (-300V)

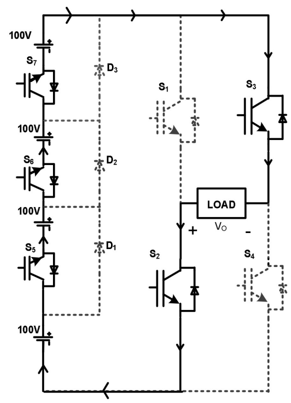

Fig. 10 (-400V)

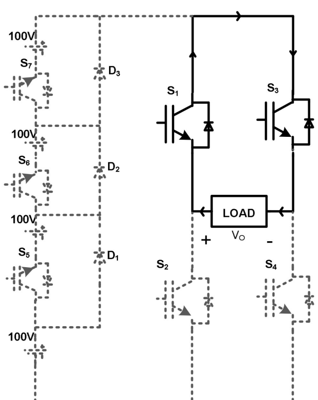

Fig. 11 (0V)

Fig. 3 to fig. 11 shows the different operating modes of the symmetrical 9-level multilevel inverter.

4. MULTI CARRIER PWM TECHNIQUES

The following section describes different multi carrier PWM techniques and can be categorized as

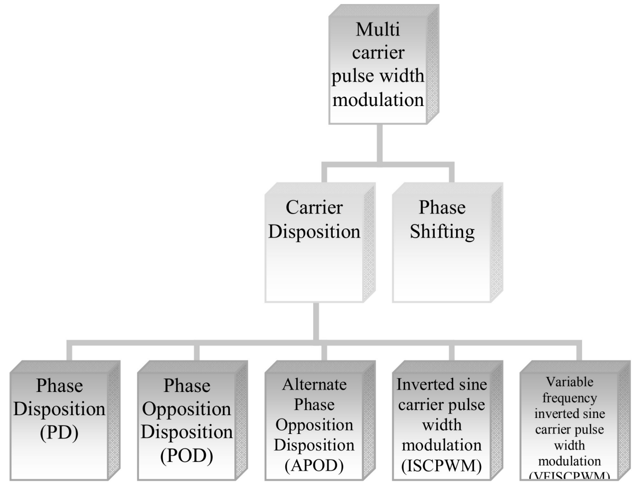

Fig. 12

4.1 CARRIER DISPOSITION

The carrier Disposition can be categorized into the following five techniques.

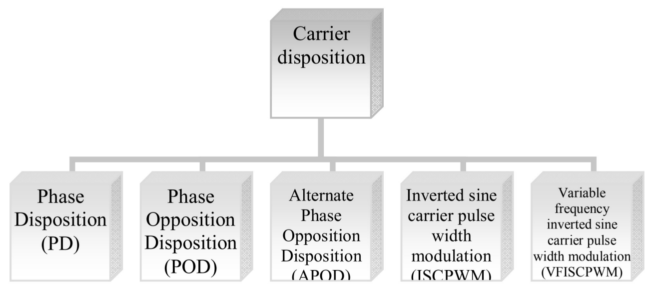

Fig. 13

These techniques are usually applied to neutral point clamped topology. These techniques may not be used for the H-Bridge inverter application directly.

4.1 (i) PHASE DISPOSITION (PD) TECHNIQUE

In this technique all carrier waveforms are superimposed over one another like layers having same phase with same amplitude and frequency but are shifted by the peak amplitude of the previous layer as shown below in the figure.

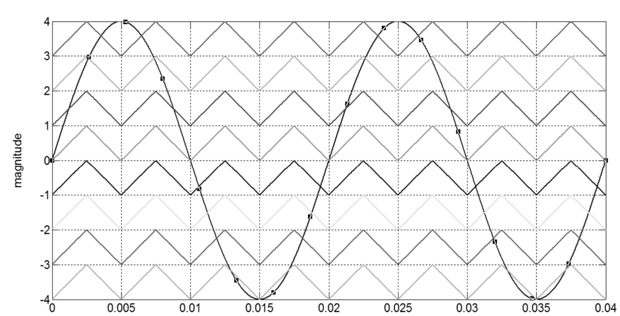

Fig. 14 PD Technique

4.1 (ii) PHASE OPPOSITION DISPOSITION (POD) TECHNIQUE

With the POD Technique the carrier waveforms above or below the zero reference value are in phase. However they are phase shifted by 180 degree between the carrier waveform above and below zero as shown in the figure below.

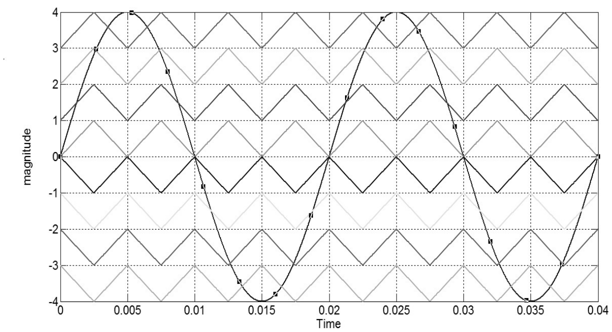

Fig. 15 POD Technique

4.1 (iii) ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) TECHNIQUE

In this technique all the adjacent carriers have a phase shift of 180 degree from each other on either side of zero reference level as shown in the figure below.

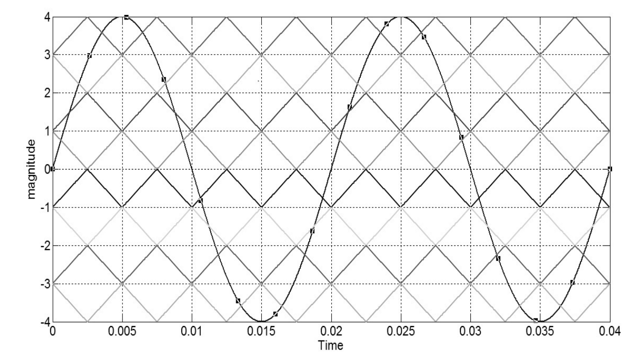

Fig. 16 APOD Technique

4.1 (iv) INVERTED SINE CARRIER PULSE WIDTH MODULATION (ISCPWM) TECHNIQUE

In this technique also sine wave is the reference signal whereas, inverted sine wave of a certain constant frequency acts as a carrier signal. Here comparison of reference and carrier signal maximize the output voltage for the given modulation index. With the help of control strategy pulses will generate whenever the amplitude of reference sine wave is greater than that of the carrier wave.

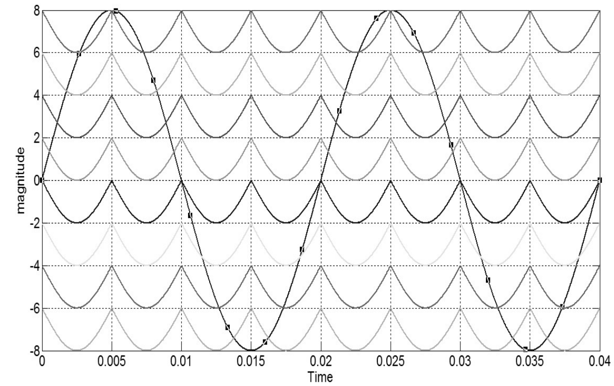

Fig. 17 ISCPWM Technique

4.1 (v) VARIABLE FREQUENCY INVERTED SINE CARRIER PULSE WIDTH MODULATION (VFISCPWM) TECHNIQUE

In this technique sine wave is the reference wave whereas inverted sine wave with variable frequency is the carrier wave here carrier signals having the multiple frequency of each other. With the help of control strategy pulses will generate whenever the amplitude of reference sine wave is greater than that of the inverted sine carrier wave.

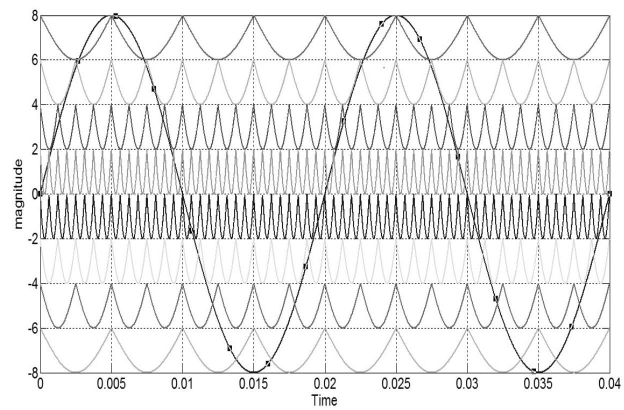

Fig. 18 VFISCPWM Technique

4.2 PHASE SHIFTING (PS) TECHNIQUE

In the phase shifted multi carrier modulation, all the triangular carriers of same frequency and identical peak to peak amplitude are shifted from its adjacent carrier by a certain angle given by $\phi = 360/(m-1)$ where m is the voltage level of multilevel inverter as shown below in the figure below.

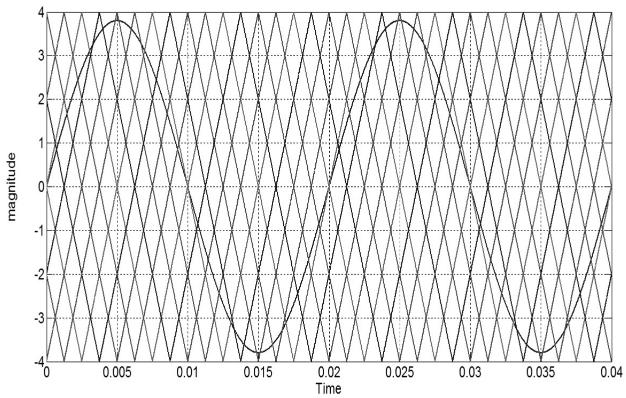

Fig. 19 PS Technique

TABLE 3 shows the comparison of THD for various modulation schemes at different modulation indices (MI) for 9 level symmetrical multilevel inverter and minimum THD is found in phase opposition disposition (POD) technique.

TABLE 3

SCHEMES	MODULATION INDICES (MI)				
	1	**0.95**	**0.9**	**0.85**	**0.8**
PD	13.81	15.74	16.30	17.19	17.31
POD	13.52	15.77	16.89	17.07	17.10
APOD	14.19	15.72	16.92	17.34	17.23
PS	13.71	15.34	17.15	16.75	20.58
ISCPWM	14.36	16.24	18.32	18.00	17.59
VFISCPWM	13.45	15.34	17.15	16.75	20.58

5. RESULTS & DISCUSSION

Several modulation techniques have been presented for Multilevel inverters such as sinusoidal PWM For the proposed structure, the fundamental frequency-switching technique is used. Since the fundamental frequency-switching technique has low-switching frequency in comparison with other strategies and it is an advantage for the power converters, THD is a popular performance index that indicates the quantity of harmonics in the output waveform. For the sinusoidal waveform, the THD varies by varying the switching angles and the number of voltage levels. It is clear that by enhancing the number of voltage levels leads to the multilevel inverter producing output waveform near to sinusoidal and as a result, very low harmonic distortion. The objective of this paper is not the calculation of the optimal switching angles in order to eliminate the selected harmonics and reducing the THD.

Fig. 20 shows the THD analysis of 9-level symmetrical multilevel inverter by phase disposition (PD) technique.

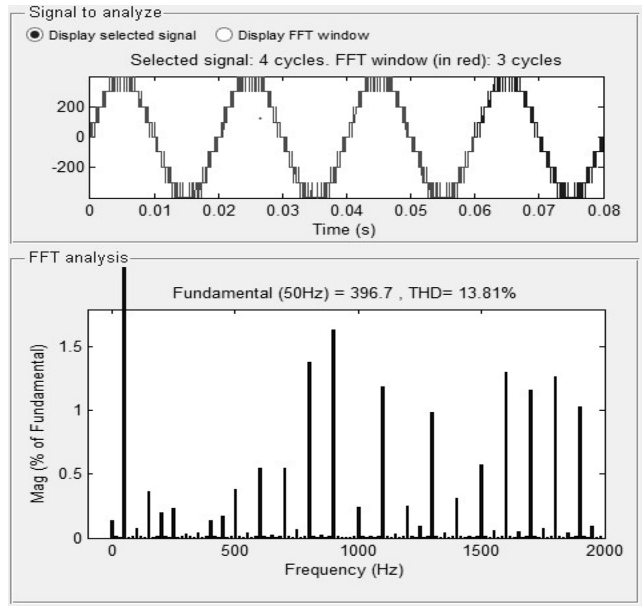

Fig. 20 THD Analysis

Fig. 21 shows the output voltage waveform of 9-level symmetrical multilevel inverter by phase disposition (PD) technique.

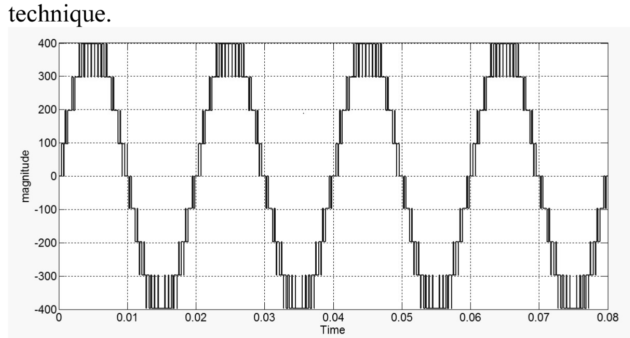

Fig. 21 Output Voltage waveform

6. CONCLUSIONS

In this paper, symmetrical multilevel inverter structures have been presented. It was shown that the proposed topology need fewer numbers of IGBTs and gate driver circuits. These factors reduce the installation area, circuit size and cost. The simulation results for a 9-level inverter based on the symmetric structure have been presented. It was shown that by applying various PWM Techniques THD of the inverter is varying, minimum THD is obtaining by Phase Opposition Disposition (POD) Technique.

7. ACKNOWLEDGEMENT

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