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A New 21- Level Asymmetrical Multilevel Inverter Topology with Different PWM Techniques

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***Abstract*—This paper presents an asymmetrical multilevel inverter topology with Different PWM techniques. This paper used one cell of conventional cascade H- Bridge Multilevel inverter structure with additional switch and voltage source to obtain high voltage level. The aim of this paper to enhance the voltage level at the output with using less switch. To improve the output voltage harmonic spectrum, the pulse width modulation (PWM) techniques used. The advantage of this proposed topology to reduce the circuit complexity and total harmonic distortion. The results of proposed 21-Level Asymmetrical multilevel Inverter are shown using MATLAB/SIMULINK software.**

Keywords— H- bridge multilevel inverter, Total harmonic Distortion (THD), Pulse width modulation (PWM).

I. INTRODUCTION

IN the last few decades the multilevel inverter widely used in electrical and electronics market due to high power and high voltage application. The multilevel comes in the existing during between the 1970s and 1980s [1]. The word multilevel inverter made from two words, first is multilevel and second is inverter. As inverter is electronics device which converts the DC Power into AC Power with desired frequency, its output has high harmonic distortion, to reduce this the output voltage level increase by which the output voltage is less distorted .The multilevel inverter starts with 3 voltage Levels.

The Multilevel inverter have an advantage over two level inverter such as, low switching losses , low switching frequency, low common mode voltage , high efficiency and better Harmonic spectrum [2-3].

The Multilevel inverter have some disadvantage also over two level inverter such as, Increasing the voltage level , the number of switches and their respective gate driver circuit increased so overall complexity of circuit increased, which increased size and cost of the circuit . So makes the balance between the desired output and cost.

The Multilevel inverter Classified on the basis of DC- voltage Magnitude are two types as Symmetrical Multilevel inverter and Asymmetrical Multilevel inverter. A symmetrical multilevel inverter have a DC-Link voltage with same magnitude and an asymmetrical multilevel inverter have a DC-Link voltage with different magnitudes. An asymmetrical multilevel inverter are classified as binary, quasi linear and ternary hybrid inverters. As compared with symmetrical configuration, an asymmetrical configuration can obtain more voltage levels in output with same number of components used in design a particular level multilevel inverter [4]. The conventional multilevel inverter can be classified as two groups, one multilevel with common dc source such as flying capacitor (FC-MLI) and diode clamped (DCMLI) and second multilevel with isolated dc source like cascade H- Bridge (CHBMLI). These structure of multilevel inverter are uses depends upon applications.

In this paper, a new asymmetrical multilevel inverter topology is proposed with a simple configuration of cascade H- Bridge multilevel inverter (CHBMLI) with reduced number of switches and insulated gate driver circuit.

In [5] a new topology of cascade H- bridge multilevel inverter has been presented. In [5], to obtain the different output voltage level, an additive and subtractive combination of voltage sources uses with one cell of cascade H-bridge multilevel inverter. This new topology with a special arrangement of voltage component that requires fewer components compared to existing conventional topology.

This paper presented a new topology for cascade multilevel inverters that produces a large number of steps with a low number of power converter switches and with different magnitudes of voltage source. In section 3, operating modes details of the proposed topology, in section 4, control and modulation techniques presented for proposed topology and Simulink results are shown in section 5.

II. PROPOSED TOPOLOGY

Fig. 1 shows the proposed topology for a 21-LEVEL Asymmetrical Multilevel inverter, which consists of the full-bridge converter with arrangement of different magnitude voltage sources and IGBT switches. In Fig.1, For 21 Level inverter 12 IGBT switches required. In this topology arrangement of different magnitude voltage sources along with full bridge converter gives the 21 level output voltage. The switches S5, S6 to S12 are used to provide the path to obtain

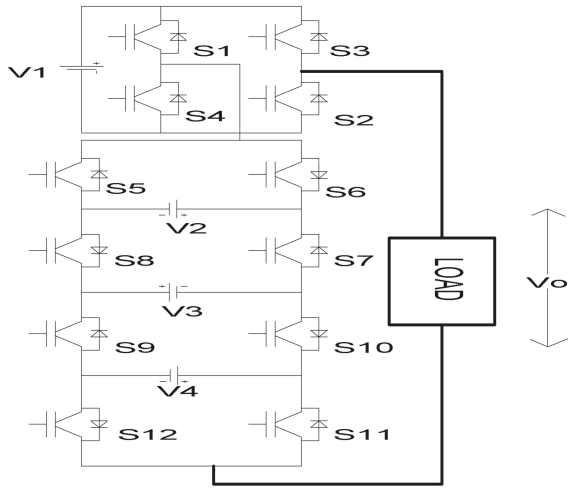


Fig.1: Proposed Topology 21- Level Asymmetric MLI

Different output voltage level. The voltage sources V1, V2, V3, and V4 are of V, 2V, 3V, and 4V respectively.

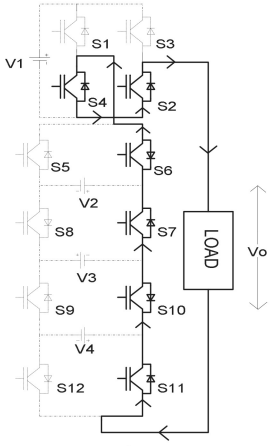
In section 3, the operating modes shows, for describes the different level output voltage. As to obtain +1 V Level, V1 and switches S3, S4, S6, S7, S10, S11 ON and Rest are OFF. Similarly +2 V, +3V and up to -10V Level obtain different switches ON and OFF, This is shown in TABLE 1.

In [5], the voltage sources V2, V3 and V4 are used for additive and subtractive the output voltage level .In table 1 shows the switching scheme of proposed Asymmetrical MLI.

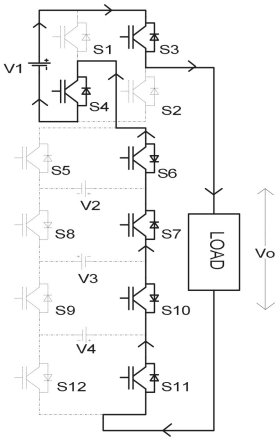
TABLE 1: SWITCHING SCHEME OF PROPOSED 21- LEVEL ASYMMETRICAL MLI

OUTPUT VOLTAGE	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+10 V	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
+9 V	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
+8 V	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON
+7 V	OFF	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON
+6 V	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF
+5 V	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON
+4 V	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON
+3 V	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
+2 V	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON
+1 V	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF
0 V	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF
-1 V	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF
-2 V	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF
-3 V	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF
-4 V	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON
-5 V	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF
-6 V	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON
-7 V	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF
-8 V	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF
-9 V	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF
-10 V	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF

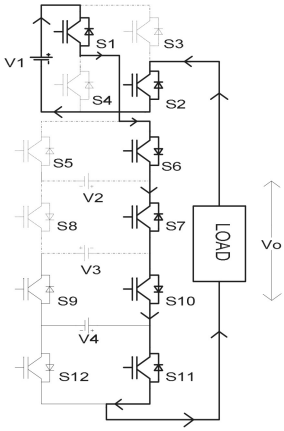
III. OPERATING MODES



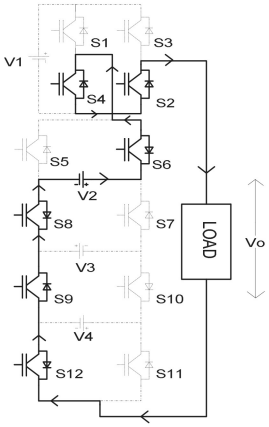
Level 0
Fig. a



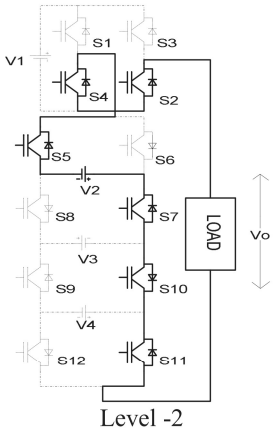
Level +1
Fig. b



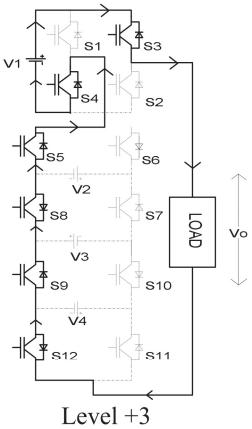
Level -1
Fig. c



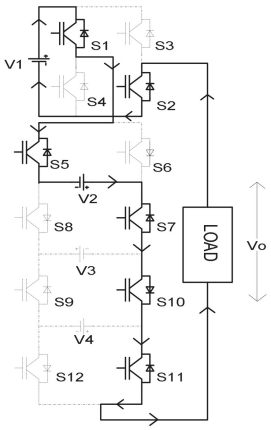
Level +2
Fig. d



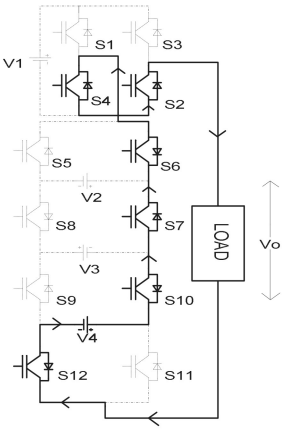
Level -2
Fig. e



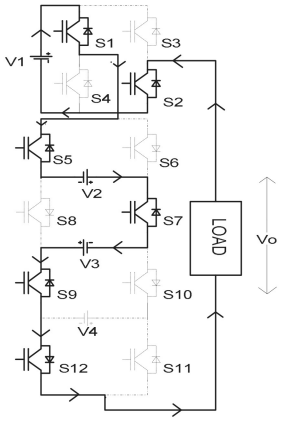
Level +3
Fig. f



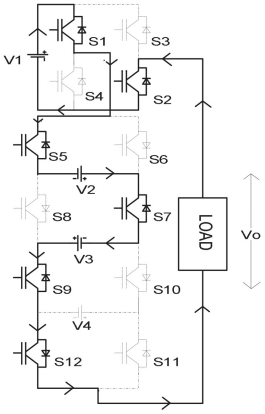
Level -3
Fig. g



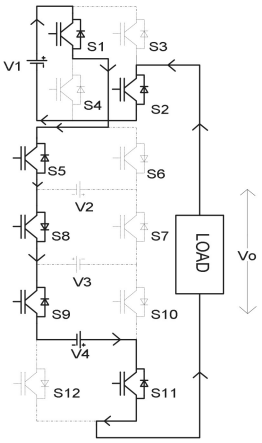
Level +4
Fig. h



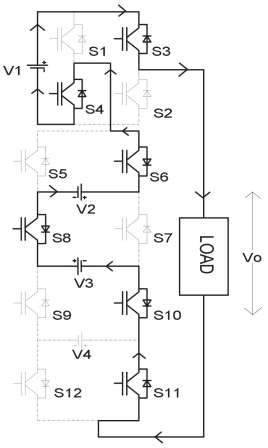
Level -4
Fig. I



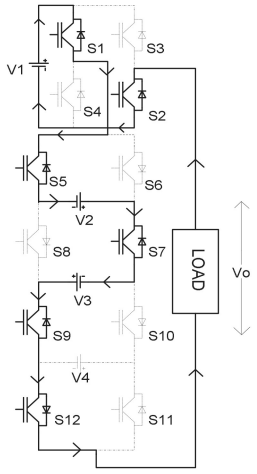
Level +5
Fig. j



Level -5
Fig. k



Level +6
Fig. l



Level -6
Fig. m

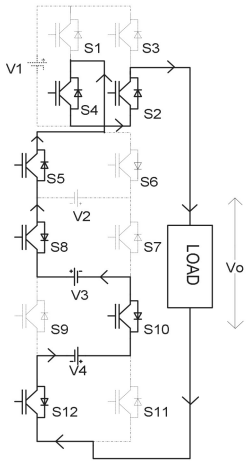


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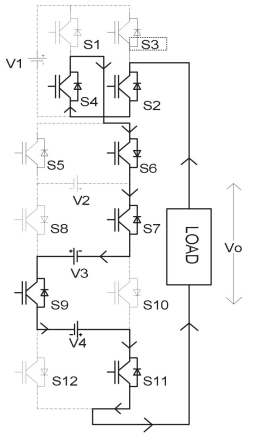
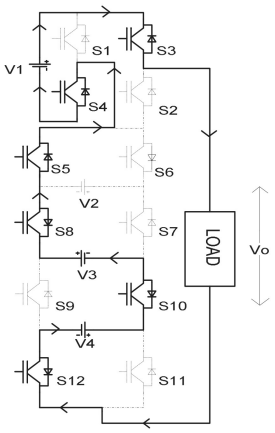
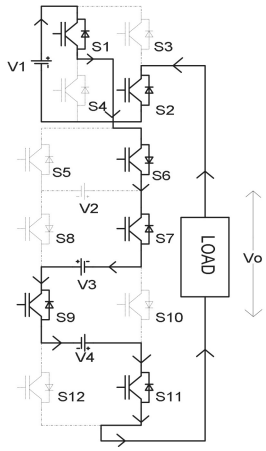
Fig. n



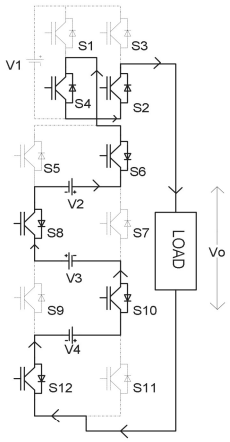
Level -7
Fig. o



Level +8
Fig. p



Level -8
Fig. q



Level +9
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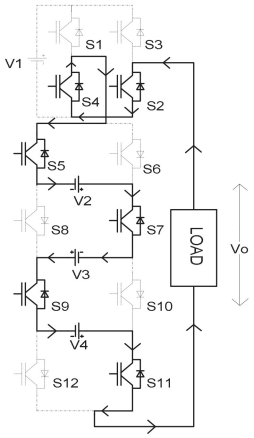
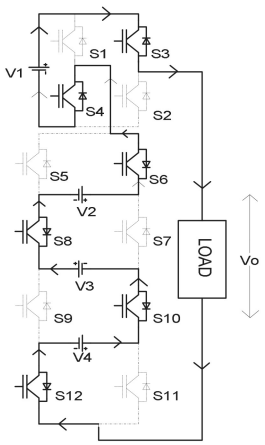
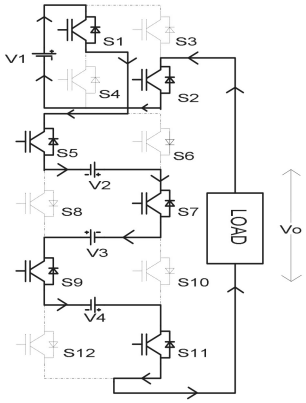


Level -9
Fig. s



Level +10
Fig. t



Level -10
Fig. u

Fig.2: Different Operating Modes of 21- Level Asymmetric MLI

TABLE 2: COMPARISION OF COMPONENTS BETWEEN PROPOSED AND CONVENTIONAL TOPOLOGIES

MLI STRUCTURE COMPONENTS	CASCADE H-BRIDGE	DIODE CLAMPED	FLYING CAPACITOR	PROPOSED TOPOLOGY
MAIN SWITCH	40	40	40	12
CLAMPING DIODES	_	380	_	_
DC SPLIT CAPACITOR	_	20	20	_
CLAMPING CAPACITOR	_	_	190	_
DC SOURCES	10	1	1	4
TOTAL	50	441	251	16

IV. CONTROL AND MODULATION TECHNIQUES

Modulation play an important role in the inverter to obtain desired output. Modulation can be over modulation and under modulation depends on modulation index. Modulation index is the ratio of reference signal to carrier signal.

In this paper multicarrier pulse width modulation (MC-PWM) technique used. As MC-PWM techniques classified as level shifted and phase shifted [6]. The level shifted multicarrier pulse width modulation techniques are as [10-11].

a) Phase Disposition (PDPWM)
b) Phase Opposition Disposition (PODPWM)
c) Alternate Phase Opposition Disposition (APODPWM)
d) Phase Opposition Disposition with variable Frequency (PODVFPWM)

a) Phase Disposition pulse width modulation (PDPWM):

In Phase disposition pulse width modulation technique all carrier above and below the zero reference are in same phase.

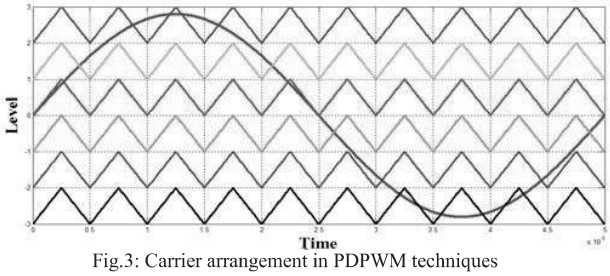


Fig.3: Carrier arrangement in PDPWM techniques

b) Phase Opposition Disposition Pulse Width Modulation (PODPWM):

In phase opposition Disposition pulse width modulation techniques all carrier above zero reference are in same phase and below the zero reference also in same phase but 180° out of phase with above the zero reference[7].

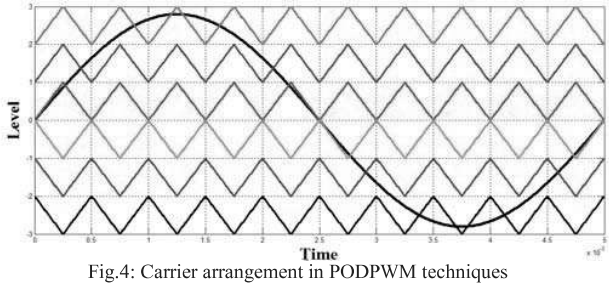


Fig.4: Carrier arrangement in PODPWM techniques

c) Alternate Phase Opposition Disposition Pulse Width Modulation (APODPWM):

In alternate phase opposition Disposition pulse width modulation scheme every carrier is out of phase with its neighbor carrier by 180° [8].

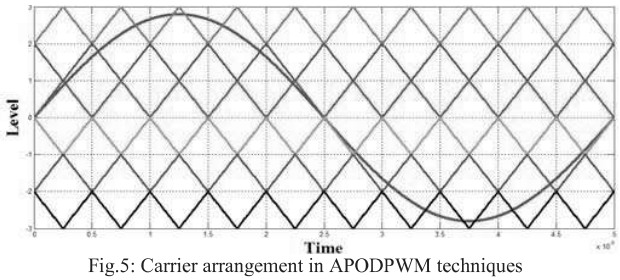


Fig.5: Carrier arrangement in APODPWM techniques

d) Phase Opposition Disposition with Variable Frequency (PODVFPWM):

In phase opposition Disposition variable frequency pulse width modulation techniques all carrier above zero reference are in same phase having different frequency and below the zero reference also in same phase with different frequency but 180° out of phase with above the zero reference [9].

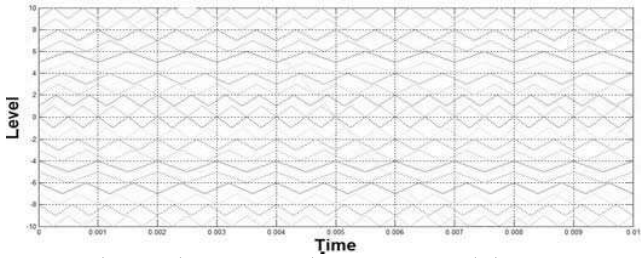


Fig.6: Carrier arrangement in PODVFPWM techniques

V. SIMULATION RESULT

To examine the performance of the proposed topology MATLAB/SIMULINK R2010 software used. In the simulation, the switches have been assumed ideal. In this paper high switching frequency method is used, switching frequency of carrier 2000 Hz. Table 3 gives the information about the Total Harmonic Distortion (THD) in 21- Level Asymmetrical Multilevel inverter with different PWM scheme and modulation index. Here some of the results are shown as.

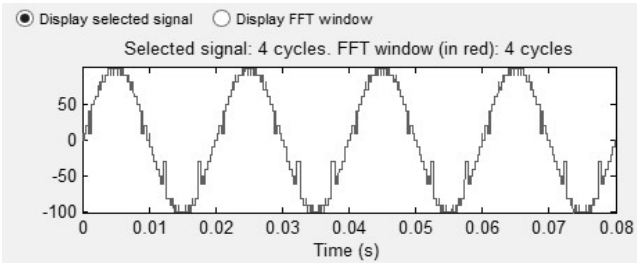


Fig.7: FFT Analysis of 21- Level Asymmetric MLI output voltage

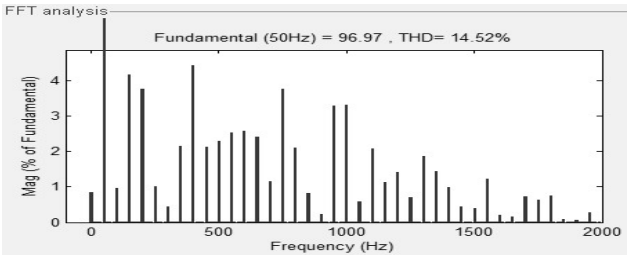


Fig.8: FFT Of 21 –Level asymmetrical MLI with PD Modulation scheme