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A New 15-Level Asymmetrical Multilevel Inverter Topology with Reduced Number of Devices for Different PWM Techniques

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***Abstract*— In this paper, a new 15-level asymmetrical multilevel inverter topology with reduced number of devices for different pulse width modulation (PWM) techniques introduces. It involves reduce number of IGBT switches, dc voltage sources, gate driver circuits used which reduces the complexity of circuit, area of installation and overall cost of system. This topology reduces total harmonic distortion (THD) of output across the load which leads to better operation of inverter and overall efficiency of system increases. The THD of the output waveform decreases as the levels of output voltage increases. Here different PWM techniques are used for multilevel inverter topology to generate 15-level output phase voltage. The output results and FFT analysis of 15-level asymmetrical multilevel inverter topology are ascertained by using MATLAB/SIMULINK software.**

***Keywords*—Multilevel inverter (MLI), pulse width modulation (PWM) techniques, total harmonic distortion**

I. INTRODUCTION

Multilevel inverter is the power electronics converter that is widely used in high power applications. In the recent years, multilevel inverters have more attention and importance in the power industry because of their high frequency and high voltage operation, low electromagnetic interference (EMI) and high efficiency [1].The thought of multilevel inverter was introduced in 1975 [2]. It basically uses several lower dc sources and then adjust a near about sinusoidal waveform [3]. Multilevel inverter gives output voltage waveform with lower harmonic distortion and as we increase the number of levels then the total harmonic distortion reduces more [4].

A multilevel inverter has several advantages over a conventional two-level inverter i.e. it generate output voltage with extremely low distortion and lower dv/dt loss across the switch i.e. efficiency increases, electromagnetic interference (EMI) and size of filter reduces, draw input current with very low distortion, generate smaller common mode (CM) voltage, MLI can operate with a lower switching frequency [1-4].

Multilevel inverter has some disadvantages over two-level inverter i.e. power semiconductor (IGBT) switches used increases which increases gate drivers that makes the system complex and costly. These disadvantages minimized by using higher number of levels in output voltage waveform.

There are three main types of conventional multilevel inverters: cascaded H-bridge multilevel inverter (CHBMLI), flying capacitor multilevel inverter (FCMLI) and diode clamped multilevel inverter (DCMLI) or neutral point clamped multilevel inverter (NPCMLI) [5]. Firstly a series connection of H-bridge inverter is known as CHBMLI was introduced in 1960s [6].Then it was followed by FCMLI topology introduced in 1992 and DCMLI topology later on evolved into neutral point clamped multilevel inverter (NPCMLI) topology [7]. But these conventional topologies have some drawbacks, in case of DCMLI topology capacitor voltage unbalancing occurs and the number of clamping diode increases as we increase the number of levels. FCMLI topology balance capacitor voltages but as we increase the number of levels, number of balancing capacitors increases and it increases the circuit complexity. CHBMLI consist of series connection of several H-bridges as we increase the number of voltage levels number of switching devices given by 2(N+1) also increases. CHBMLI requires separate dc source, hence renewable energy sources can be utilized as input for this topology. But it reduces its area of applications [8].

Here a new 15-level asymmetrical multilevel inverter topology based on series connected dc sources has been proposed. It requires less number of switches, number of driver circuits and number of dc sources used. It also reduces total harmonic distortion (THD). The THD of proposed topology is compared with different PWM techniques.

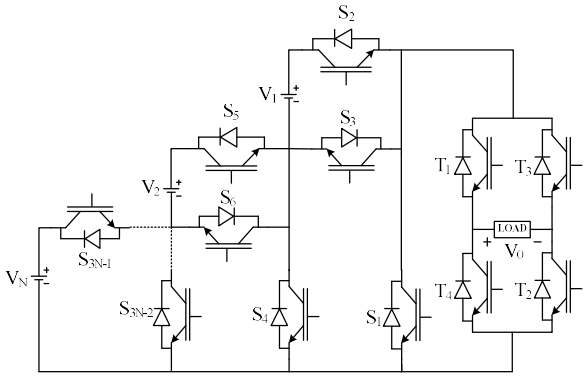

Fig.1. Proposed Topology.

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