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978-1-5386-6472-8/18/$31.00 ©2018 IEEE

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Design and Analysis of a New 31-Level Asymmetrical Multilevel Inverter Topology with Different PWM Techniques

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***Abstract*— This paper presents an asymmetrical multilevel inverter topology with different pulse width modulation technique. The main objective of this paper is to increase the number of levels at the output voltage with less switches used. This proposed topology offers high power capability associated with less commutation losses, less total harmonic distortion (THD), and involves less number of switching devices and less number of voltage source in comparison of conventional topologies for 31-Level asymmetric multilevel inverter. This topology used asymmetric voltage sources is in nature, that required four asymmetric voltage sources and ten switching devices for producing 31-Level single phase output voltage. This paper presents the comparison of total harmonic distortion for different pulse width modulation technique, with different modulation index, and the simulation result of proposed topology for single phase 31-level multilevel inverter, which are carried out by using MATLAB/Simulink R2013a software version.**

Keywords—Asymmetric Multilevel Inverter (ASMLI), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD).

I. INTRODUCTION

Inverter is an electrical device which converts direct current (DC) to alternate current (AC). Multilevel inverter is an extended form of an inverter, which appears in power electronics systems in 1975, because of the requirement of the good quality of power, with better system efficiency [1]. Multilevel inverters becomes more popular over the years in high power medium voltage application because of its capability of handling the high power with less harmonic distortion (THD), good power quality, and reduced switching losses. When the level of output voltage increases the harmonics in the output voltage decreases. Two level inverter produces two levels ($+V_{DC}$ and $-V_{DC}$) in output, and Multilevel inverter is used to provide more than two voltage level at output, to achieve smoother and less distorted DC to AC power conversion at desired AC output voltage and it can generate a multiple step voltage waveform with less distortion and higher efficiency [5].

As compare with the two level inverter, Multilevel inverter have several advantages like lower commutation losses that's why the efficiency is improved, less dv/dt stress across the switch, lower harmonic contents, lower electromagnetic interference (EMI), and filter size is also reduced [2][3][4]. Multilevel inverter also have some disadvantages that is large number of power electronic switching devices required, with respective gate driver circuits, which makes the configuration complex and system costly [6].

The general concept of multilevel inverter is, utilizing a more number of semiconductor switches to perform the power conversion in small voltage steps. There are mainly three types of conventional multilevel inverter, Diode Clamped multilevel inverter (DCMLI) [7], Flying Capacitor multilevel inverter (FCMLI) [3], and Cascaded H-Bridge (CHB) multilevel inerter [8]. In DCMLI topology, as the number of levels in voltage increased, more number of clamping diodes required. In FCMLI topology, as the number of levels in voltage increased, more number of flying capacitor required. CHB multilevel inverter topology is the simplest topology among the all conventional topologies. In CHB multilevel inverter topology, clamping diodes and flying capacitors are not required, but as the number of levels in voltage increased, more number of DC voltage sources required.

Generally, Cascaded H-Bridge multilevel inverters can be classified in two types: Symmetric and Asymmetric multilevel inverters. When the value of DC voltage sources in H-bridges are equal, is called Symmetric multilevel inverters. When the value of DC voltage sources in H-bridges are unequal, is called Asymmetric multilevel inverter. Asymmetrical topologies required less switching devices and voltage sources as compared to symmetrical topologies for same levels in output voltage. This paper proposed a topology for 31-Level asymmetrical multilevel inverter, which required less number of switching devices in comparison with conventional topologies [4], shown in Table III. This paper used different pulse width modulation techniques (PWM) with different modulation index to analyze total harmonic distortion (THD) in the output voltage waveform.

II. PROPOSED TOPOLOGY

This paper presents a new topology based on asymmetrical multilevel inerter (ASMLI), shown in Fig. 1, which required four unequal voltage sources (V_1, V_2, V_3, and V_4) and ten unidirectional switches (S_1, S_2, S_3, S_4….. S_{10}), which is combination of IGBT with antiparallel Diode, for 31 levels in output voltage of proposed asymmetric multilevel inverter. For 31-Level MLI, proposed topology produces maximum voltage ($V_4 + V_3$).

From Fig. 1, it is clear that switching combination of (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8), and (S_9, S_{10}) should not be turned 'ON', simultaneously, to avoid short circuit across the voltages. To generate all the positive and negative levels in the output voltage, magnitude of the voltage sources

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