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Reduced Device Count Asymmetrical Multilevel Inverter Topology Using Different PWM Techniques

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***Abstract*-- This paper presents a new topology in a multilevel inverter (MLI) field with reduce device count and less number of dc voltage source with different PWM technique. This Proposed topology offers high power capability associated with less commutation losses, less total harmonic distortion (THD). For a specific number of levels in output, proposed topology required less switching components and DC voltage sources in comparison of Conventional topologies. This topology used asymmetric voltage sources is in nature, that required three asymmetric voltage sources and eight switching devices for producing 15-Level single phase output voltage. This topology is simple and optimal, which can be easily extended for higher level in output voltage of multilevel inverter. This paper presents the comparison of total harmonic distortion, with different pulse width modulation technique, with different modulation index, and the simulation result of proposed topology for single phase 15-level multilevel inverter, which are carried out by using MATLAB/Simulink R2013a software version.**

Keywords— Multilevel Inverter (MLI), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD)

I. INTRODUCTION

Multilevel inverter (MLI) is an extended form of an inverter, which appears in power electronics systems in 1975, because of the requirement of the good quality power, with better system efficiency [1]. Multilevel inverters becomes more popular over the years in high power medium voltage application because of its capability of handling the high power with less harmonic distortion (THD), reduced switching losses and good power quality. As the number of levels in output voltage waveform increases, harmonics in the output voltage waveform decreases. In comparison with two level inverter, multilevel inverter has several advantages like lower commutation losses that's why efficiency is improved, less dv/dt stress across the switch, lower harmonic contents, lower electromagnetic interference (EMI), and reduced filter size [2][3][4]. In multilevel inverter (MLI) requirement of power electronics switching components is more, which makes configuration complex and costly [5], can be considered as a disadvantage of MLI.

Multilevel inverter is used to generate a multiple step output waveform, to achieve smoother and less distorted DC to AC power conversion at desired AC output voltage [6]. The general concept of multilevel inverter is, utilizing a more number of semiconductor switches to perform the power conversion in small voltage steps. There are mainly three types of conventional multilevel inverter, Diode clamped multilevel inverter (DCMLI) [7], Flying capacitor multilevel inverter (FCMLI) [2], and cascaded H-bridge (CHB) multilevel inerter [8]. In DCMLI topology, as the number of levels in voltage increased, more number of clamping diodes required. In FCMLI topology, as the number of levels in voltage increased, more number of flying capacitor required. CHB multilevel inverter topology is the simplest topology among the all conventional topologies. In CHB multilevel inverter topology, clamping diodes and flying capacitors are not required, but as the number of levels in voltage increased, more number of DC voltage sources required.

Generally, CHB multilevel inverters can be classified in two types: Symmetric and Asymmetric multilevel inverters. When the value of DC voltage sources in H-bridges are equal, is called Symmetric multilevel inverters. When the value of DC voltage sources in H-bridges are unequal, is called Asymmetric multilevel inverter. Asymmetrical topologies required less switching devices and voltage sources as compared to symmetrical topologies for same levels in output voltage. This paper proposed a topology for Asymmetrical multilevel inverter, which required less number of switching devices in comparison with conventional topologies [4]. For 15-Level MLI total device count required in proposed topology is compared with conventional topologies, shown in Table III. This paper used different pulse width modulation techniques to analyze total harmonic distortion in the output voltage waveform.

II. PROPOSED TOPOLOGY

This paper proposed a topology based on asymmetrical multilevel inerter, shown in Fig. 1, which required N unequal voltage sources (V_1, V_2, V_3….. V_N) and (2N+2) unidirectional switches (S_1, S_2, S_3, S_4….. $S_{(2N+2)}$), for (2^N-1) levels in output voltage of proposed multilevel inverter. Generally, the proposed topology produces maximum voltage ($V_n + V_{n-1}$). The proposed topology starts with 7 level, for which two unequal voltage sources and six unidirectional switches, consists of IGBT with an antiparallel diode, required. For generating all positive and negative levels, magnitude of voltage sources (V_1:V_2) should be in the ratio of (1:2).

To generate 15-Level MLI, proposed topology required three unequal voltage sources and eight unidirectional switches, shown in Fig. 2, it is clear that switching combination of (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) should not be turned 'ON', simultaneously, to avoid

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